

PGY-UFS 4.0-PA MPHY, UniPro, UFS Protocol Analyzer



PGY-UFS4.0-PA, UFS Protocol Analyzer is the industry first working and tested UFS4.0 Protocol Analyzer. It offers protocol data capture and debug of data across MPHY, UniPro and UFS protocol layers. It allows for instantaneous decoding of UFS, UniPro and MPHY layers with flexibility to correlate decoded data across these protocol layers. PGY-UFS4.0-PA supports PWMG1 to HSG5B data rates and two TX, two RX lane decode. The active probe has minimum electrical loading on device under test (DUT) and captures protocol data without affecting the performance of DUT. PGY-UFS4.0-PA Protocol Analyzer support two lane data. Comprehensive on the fly decoding of UniPro & UFS data enables validation of communication between UFS host and device.

PGY-UFS4.0-PA Protocol Analyzer allows Design and Test Engineers to obtain deep insight into UFS host and device communication. MPHY/UniPRO/UFS packet-based triggering allows specific protocol data capture and analysis. PGY-UFS Protocol analyzer instantaneously provides decoding of UFS, UniPro and MPHY layers with a correlation to MPHY, UniPro and UFS layers.

Solder down active probes allows probing the MPHY test points. This allows the design and test engineers to capture UFS traffic between the host and UFS memory with high signal fidelity. Today's test engineers need to test the use case scenarios in their labs that mimic real-life use cases. The PGY-UFS4.0-PA, UFS Protocol Analyzer has been designed to enable engineers to closely monitor and analyze the traffic between the host and the device while executing the various use case scenarios.

PGY-MPHY-UniPRO-UFS Protocol Analysis Software

File Setup View Trigger Analytics Report Help

Connect Acquire Stop Acq Stop Transfer Stop Reset UPRO_Mkr Δt1 M0 M1 - 170.2375ms Δt2 M0 M1 - 170.2375ms UFS_Mkr Δt1 P0 P1 - 348.5025ms Δt2 P0 P1 -

UFSView	DeviceConfigView	Analytics View	PacpView	Report View	TriggerView	Color Settings	SymbolsView_HOST	SearchView		
Index	Timestamp	Host	Device	Gear	Task Tag	Total EHS Length	Segment Length	Data Offset	LUN	Status
9	531.9985ms	WRITE_10	RESPONSE	HS_G5B	03	00	0000		01	Good
10	648.9097ms	WRITE_10	HS_G5B	04	00	0000			01	
11	673.8643ms	READY_TO_TRANSFER	HS_G5B	04	00	0000			01	
12	702.2748ms	DATA_OUT	HS_G5B	04	00	1000		00000000	01	
13	702.2782ms	RESPONSE	HS_G5B	04	00	0000			01	Good
14	777.6731ms	READ_10	HS_G5B	05	00	0000			01	
15	827.1691ms	DATA_IN	HS_G5B	05	00	1000		00000000	01	
16	827.1709ms	RESPONSE	HS_G5B	05	00	0000			01	Good
17	944.0402ms	WRITE_10	HS_G5B	06	00	0000			01	
18	968.9898ms	READY_TO_TRANSFER	HS_G5B	06	00	0000		15	01	
19	997.4088ms	DATA_OUT	HS_G5B	06	00	1000		00000000	01	
20	997.4122ms	RESPONSE	HS_G5B	06	00	0000			01	Good
21	1.072827s	READ_10	HS_G5B	07	00	0000			01	

UniProView	Index	Timestamp	Host	Device	Gear	DestDeviceID	DestPortID	EOM	Frame Seq	Credit Value	CRC
H2	1381	997.4094ms	DL_DATA	HS_G5B	01	00	00	00			
	1382	997.4094ms	DL_AFC	HS_G5B				07	9B		
	1383	997.4096ms	DL_AFC	HS_G5B				08	A4		
	1384	997.4096ms	DL_DATA	HS_G5B	01	00	00	0A			
	1385	997.4098ms	DL_AFC	HS_G5B				09	AC		
	1386	997.4099ms	DL_DATA	HS_G5B	01	00	00	00			
	1387	997.4102ms	DL_AFC	HS_G5B				0A	B5		
	1388	997.4101ms	DL_DATA	HS_G5B	01	00	00	0C			
	1389	997.4102ms	DL_AFC	HS_G5B				0B	BD		
	1390	997.4103ms	DL_DATA	HS_G5B	01	00	00	0D			
	1391	997.4105ms	DL_AFC	HS_G5B				0C	C6		
	1392	997.4103ms	DL_DATA	HS_G5B	01	00	00	0E			
	1393	997.4107ms	DL_AFC	HS_G5B				0D	CE		

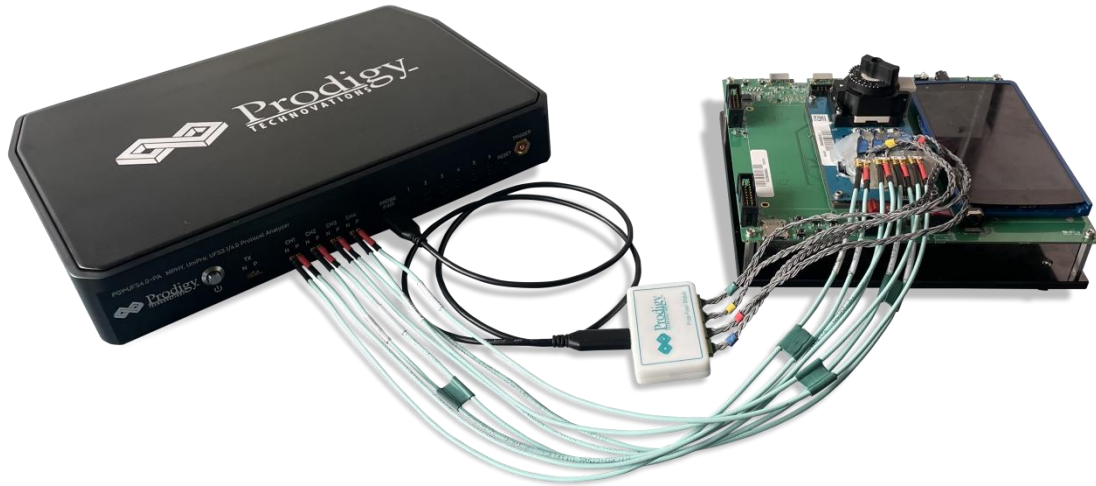
1.3.7.0 Received: 0 Current Mem: 0.000GB Max Mem: 0.000GB HSG5B_2 Analysis Completed..

Windows based protocol analysis software provides industry best protocol correlation between UFS to UniPro and MPHY layers. Time correlation between the different protocol layers significantly reduces debug time of designs. Floating window design of this software allows engineers to view UFS view, UniPro view and MPHY view on different computer monitors and automatically correlate the UFS packets to MPHY layer. This makes analysis very easy while analyzing the gigabytes of Protocol information.

Key Features

- ❖ Supports version MPHY 5.0, UniPro 2.0 and UFS v2.1/3.1/4.0
- ❖ Supports PWM G1 to G7 and HS G1, 2, 3, 4, 5 Rate A and B Series (up to 23.32Gbps)
- ❖ Supports one/two data lanes (2 TX and 2 RX)
- ❖ Flexibility to capture very large data using continuous streaming of Protocol data to host computer with 16GB Internal acquisition memory field upgradable up to 64GB.
- ❖ Hardware based resizable circular buffer with pre/post trigger.
- ❖ Flexibility to decode selected data from 16GB buffer.
- ❖ Solder down active probe provide high signal fidelity.
- ❖ Decoding at MPHY, UniPro and UFS layers.
- ❖ Trigger based on MPHY, UniPro and UFS layers packet content.
- ❖ Trigger out signal at trigger event allows the triggering of other instruments such as oscilloscope.
- ❖ Interface to host system using USB 3.0.
- ❖ Flexibility to upgrade the hardware firmware using GbE interface provides easy field up gradation of FPGA firmware.
- ❖ Decoded data packets can be exported to txt file for further analysis.
- ❖ Light weight and can be deployed for on-site/ field tests.
- ❖ Regulatory CE marked and RoHS compliant

Test Setup



PGY-UFS4.0-PA UFS Protocol Analyzer interfaces to solder down probe tips using mSMP flexi coax cables. The active probe tips are powered by power module which is powered by PGY-UFS4.0-PA. Protocol Analyzer is interfaced to host computer using USB3.0 interface. High-speed host connectivity and 16GB buffer enables continuous streaming of protocol data to host SSD and storage for longer period of time. Software offers multi-view such as MPHY view, UniPro view and UFS View. Each view lists the respective protocol packets and its details with correlation of each layer for easy debug. Lightweight Analyzer is easy to carry during field visit.

Advanced Settings

Burst Speed Detection		Sync Wait Time		Host		Device	
<input type="radio"/> Sync Speed		Host	10	CTLE	MANUAL	Freq Boost	5
<input checked="" type="radio"/> PACP PWR Gear		Device	32	DFE Gain	MANUAL	Wide Band Gain	7
				DFEGain CFG	31	DFE Gain	MANUAL
				DFEGain CFG	31	DFE Gain	MANUAL

Acquisition/Error Analysis

Analyze	Hardware Filters	Buffer Type	CRC Error Count
<input type="radio"/> Live Decode	<input checked="" type="checkbox"/> AFC	<input checked="" type="radio"/> Continuous/8GB	<input type="checkbox"/> DLData
<input checked="" type="radio"/> Post Capture	<input type="checkbox"/> DLData Payload Drop	<input type="radio"/> Circular (H/W)	<input type="checkbox"/> AFC
		Buffer Size	
		PreTrigger	
		0 MB	
		0 100	

UFS Protocol Layer

Index	Timestamp	Host	Device	Gear	Task Tag	Total EHS Length	Segment Length	Data Offset	Expected D	Logical Block Adc	Device Int	Transfer Le	Response
..7809	17.45788104s	READ_10		HS_G4B	03	00	0000		00001000	005E2886		0001	
..7810	17.457897816s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7811	17.457899632s		RESPONSE	HS_G4B	00	00	0000						Success (00)
..7812	17.457913712s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7813	17.457915536s		RESPONSE	HS_G4B	02	00	0000						Success (00)
..7814	17.457919936s	READ_10		HS_G4B	01	00	0000		00001000	005E5B72		0001	
..7815	17.457937432s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7816	17.457938208s	READ_10		HS_G4B	00	00	0000		00001000	005D0F2E		0001	
..7817	17.457939264s		RESPONSE	HS_G4B	03	00	0000						Success (00)
..7818	17.457974088s	READ_10		HS_G4B	02	00	0000		00001000	005E707A		0001	
..7819	17.457979048s		DATA_IN	HS_G4B	01	00	1000	00000000					
..7820	17.457980872s		RESPONSE	HS_G4B	01	00	0000						Success (00)
..7821	17.457981648s	READ_10		HS_G4B	03	00	0000		00001000	005E2517		0001	
..7822	17.457994964s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7823	17.457996808s		RESPONSE	HS_G4B	00	00	0000						Success (00)
..7824	17.458019368s	READ_10		HS_G4B	01	00	0000		00001000	005E5B7C		0001	
..7825	17.458031576s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7826	17.458031672s	READ_10		HS_G4B	00	00	0000		00001000	005DAD56		0001	
..7827	17.4580334s		RESPONSE	HS_G4B	02	00	0000						Success (00)
..7828	17.458037632s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7829	17.458039448s		RESPONSE	HS_G4B	03	00	0000						Success (00)
..7830	17.458073704s	READ_10		HS_G4B	02	00	0000		00001000	005E8D79		0001	
..7831	17.458076264s		DATA_IN	HS_G4B	01	00	1000	00000000					
..7832	17.458078088s		RESPONSE	HS_G4B	01	00	0000						Success (00)
..7833	17.458083496s	READ_10		HS_G4B	03	00	0000		00001000	005E0192		0001	
..7834	17.458087656s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7835	17.45808948s		RESPONSE	HS_G4B	00	00	0000						Success (00)
..7836	17.458116096s	READ_10		HS_G4B	01	00	0000		00001000	005E52A4		0001	
..7837	17.458127792s	READ_10		HS_G4B	00	00	0000		00001000	005D8026		0001	
..7838	17.45813994s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7839	17.458132224s		RESPONSE	HS_G4B	02	00	0000						Success (00)
..7840	17.458140168s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7841	17.458141992s		RESPONSE	HS_G4B	03	00	0000						Success (00)
..7842	17.458170272s	READ_10		HS_G4B	02	00	0000		00001000	005E7F40		0001	

PGY-UFS4.0-PA Software can display each UFS packet parameters in a listing window. Right click lists all the packet parameter for user selection. User can color code the fonts or background color for easy identification for each UFS packet.

PACP And Unipro View

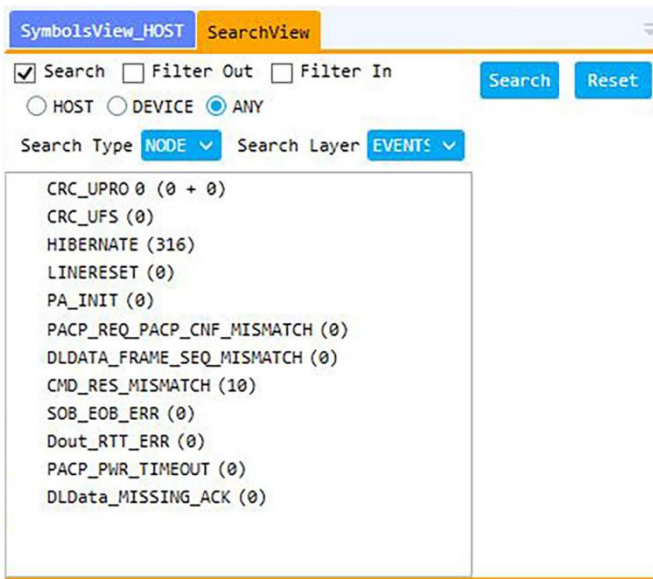
The screenshot displays the PGY-MPHY-Unipro-UFS Protocol Analysis Software interface. The main window is divided into several panes:

- Connection View:** Shows connection parameters like UPRO_Mkr, M0, M1, and UFS_Mkr.
- PACPView:** A table showing PACP packets with columns for Index, Timestamp, Direction, Description, Gear, Tx Lane, Tx Mode, Rx Lane, Rx Mode, Flags, CRC, MIBattribut, MIBvalue, and LineReset. It lists various PACP_PWR_req and PACP_PWR_cnf packets.
- UniProView:** A table showing UniPro packets with columns for Index, Timestamp, Host, Device, Gear, Flags, EOM, Frame Seq, Credit Value, and CRC. It lists packets like DL_AFC, PACP_PWR_req, PACP_PWR_cnf, and EOB.
- SymbolsView_HOST and SymbolsView_DEVICE:** Additional views showing packet details for the host and device respectively.

At the bottom, the software status shows: 1.2.8.0, Received: 0, Current Mem: 0.000GB, Max Mem: 2.839GB, and Analysis Completed.

PGY-UFS4.0-PA Software separates the PACP packets in a separate view for easy analysis of power mode change packets and link to UniPro packets. Users can view the MPHY states stall, prepare, sync information in UniPro view apart from user selection for DL_Data and AFC/NACK Packet details.

Error Events, Search and Filter



PGY-UFS3.X-PA Software does the live decode and list all the events. The list of events are shown in this picture. Users can easily note the errors in captured protocol data. In large buffer capture, it takes extremely difficult to locate the errors. But PPGY-UFS3.X-PA software simplifies this by listing events while decoding the captured data. Search and Filter allows you directly locate the error events or UFS or UniPro or PACP packet in the protocol listing windows. Filter-in and Filter-out makes it easy view the data of interest in the protocol listing window.

Comprehensive Protocol Analysis Using Multi-View



PGY-UFS4.0-PA UFS Protocol Analyzer provides USB3.0 interface for host computer connectivity. High-speed host connectivity enables continuous streaming of protocol data to host HDD and storage for long period of time. Software offers multi-view such as MPHY view, UniPro view and UFS View. Each view lists the respective protocol packets and its details with correlation of each layer for easy debug.

PGY Protocol Analyzer's easy to use interface, reduces the protocol analysis time. Time stamped view of protocol decode listing provides easy view of protocol activities between host and the device. At a click of a button, user can view the decode of each packet and the intended function. Floating window software architecture allows the user to view each protocol layer on separate monitors for easy debug. Autocorrelation of each selected packet from UFS to MPHY layers simplifies the debug activity

Specifications

Data Rates Supported	PWM G1 to G7, High Speed Gear 1, Gear 2, Gear 3 and Gear 4, Rate A and B, Gear 5 Rate A and B
Link width	Configurable for 1TX/1RX or 2TX/2RX
Lanes supported	Two data lanes (2 TX and 2 RX)
Probes	Solder Down Active Probes (Standard) CTLE Probes(Solder Down/mSMP) , Power Divider , Raised PCB Interposer
Protocol Decode	UFS, MPHY and UniPro layers
Protocol supported	UFS v2.1/v2.2/3.1/4.0 MPHY 3.0/4.0/4.1/5.0 UniPro 1.6/1.8/2.0
Signal swing	400mV
Trace Capture Size	Supports Continuous streaming of Protocol data to Host computer SSD/HDD. Internal acquisition memory of 16GB expandable up to 64GB
Trigger	Based MPHY, UniPro, UFS Packets
Front Panel Connectors	Interface for Active probes. Trigger in/out SMA connectors
Interface for Host Computer	USB3.0 and Gigabit Ethernet interface
Host Computer Requirements	Windows 7/8.0/8.1/10 64bit operating System. It supports a RAM of minimum 8GB, but the product would give a faster response for a 32GB. The minimum storage capacity of 100GB should be available in the hard disk drive. User can use more storage based on trace storage requirement. Display resolution of the monitor is 1024X768. Host computer should support USB3.0 or GBe interface.
Temperature (Operating) (Non - Operating)	+0 °C to +50 °C (32 °F to 122 °F) -20 °C to +60 °C (-4 °F to 140 °F)
Dimension	(W x H x D) (20.5X5X25) cms
Weight	Approx. 2.5Kg
Power Requirement	12V, 3A DC Power Supply (AC/DC Supplied along with Analyzer)
ESD	Regulatory CE marked and RoHS compliant

Trigger Specifications

Stack	Protocol Analyzer	Packet Type
	Link Start-up Sequence	(TRG_UPRO0)
		(TRG_UPRO1)
		(TRG_UPRO2)
UniPRO	PHY Capability Adapter Packets (PCAP)	PACP_PWR_reg
		PACP_PWR_cnf
		PAC_Cap_ind
		PACP_Cap_EXT1_ind
		PACO_EPR_ind
		PACP_TestMode_req
		PACP_GET_req
		PACP_GET_cnf
		PACP_SER_req
		PACP_SET_cnf
		PACP_TEST_Data_0
		PACP_TEST_Data_1
		PACP_TEST_Data_2
PACP_TEST_Data_3		
	Data Link Packets	SOF
		EOF
		EOF_ODD
		EOF_EVEN
		COF
		AFC/NAC
		Traffic class 0/Traffic class 1
UFS	UFS Layers Packets	NOP IN
		NOP OUT
		Commands
		Response
		Task Management Request
		Task Management Response
		Ready To Transfer
		Ready to Transfer

UFS Probing Solutions



P4012 - HSG5B (23.32Gbps) Solder-in probetips

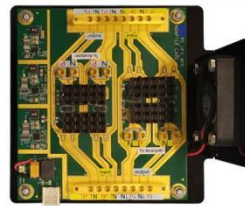


P4012 - SMPM probe tips



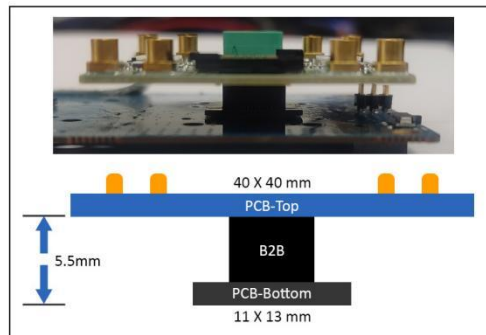
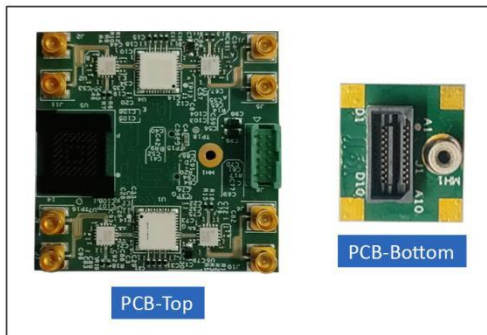
P4012-CTLE-mSMP
(UFS4.0 Compatible mSMP Probe tips with CTLE)

P4012-CTLE
(UFS4.0 Compatible Solder Probe tips with CTLE with sense resistor connected.)



P4012-INT-mSMP
mSMP Power divider Interposer PCB with integrated probe tip

UFS4.0 Compatible CTLE Probe tips



P4012-INT-B2B

UFS 4.0 Board to Board Interposer with Integrated probe tips with the P4012-INT-B2B-PCB - Bottom PCB

Probing UFS signal is one of the key challenges in reliable UFS protocol decode. In most of the DUT, test points are located close to each other without enough space to solder the probe tips. Solder-in probe tips that can be soldered directly to test pads between the UFS host and device. This probe tip has high analog bandwidth to boost the HSG5B (23.32Gbps) signals. Active circuit in probe tip efficiently drives the low power MPHY signal to UFS 4.0 Protocol Analyzer for error free Protocol Analysis at UFS 4.0 speeds. Many of the UFS 4.0 development platforms have SMPM connector to access the MPHY Signals. To probe such device, Prodigy Technovations offers SMPM probe tips. SMPM probe tips has mating SMPM connector with DUT. This makes it convenient connect to the DUT and analyze UFS 4.0 Protocol data. SMPM coaxial cables are required to connect the power divider to UFS test setup. These cables are to be separately arranged by user.

Ordering Information

Part no	Product Description
PGY-UFS4.X-PA	UFS4.0 Protocol Analyzer supports HSG5B rate (with full backward compatibility to UFS2.0/2.1/3.0/3.1)
<i>Standard Bundle:</i>	
PGY-UFS4.X-PA SW	PGY-UFS-PA Software
P6011A	mSMP Coax Cables (0,5 mtr long) - Pair
P4012	UFS4.0 Compatible solder Probe tips (4qty)
3210	LAN cable
3220	USB Cable
4240	12V DC Power Adapter for UFS4.0

Optional Probes

P4012	UFS4.0 Compatible solder Probe tips (4qty)
P4012-mSMP	UFS4.0 Probe Tips with mSMP connector (4qty)
P4012-CTLE	UFS4.0 Compatible mSMP Probe tips with CTLE (2qty) Note: Probe tips with Continuous Time Linear Equalizer - CTLE , Can supports 2 lanes, 2TX or 2RX
P4012-CTLE-mSMP	UFS 4.0 Compatible mSMP Probe tips with (2qty) Note: Probe tips with Continuous Time Linear Equalizer - CTLE , Can supports 2 lanes, 2TX or 2RX Included: P6012 - MSMP RA (F) to MSMP (F) Flexi Cable (39mm)-4 Pairs
P4012-INT-mSMP	mSMP Power divider Interposer PCB with integrated probe tip Note: Connection cables to be purchases by end user based on the connector on thier end.
P4012-INT-B2B	UFS4.0 Board to Board Interposer with integrated probe tip Note: Connection cables to be purchases by end user based on the connector on their end.
P4012-INT-B2B-PCB	Base PCB for UFS4.0 Board to Board Interposer

Warranty Information

12 months return to Prodigy hardware warranty from the date of delivery.

12 months software update support from date of delivery.

Note: Probes, cables & accessories carry 90 days warranty for any manufacturing defects only.

Contact Information



+91-80-42126100



contact@prodigytechno.com



www.prodigytechno.com



Prodigy Technovations Pvt. Ltd.

294, 3rd Floor, 7th Cross,
7th Main BTM II Stage,
Bangalore 560076.
Karnataka, India.

About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.