



PGY-SSM-EV-Tester

SD and eMMC AC/DC Electrical Characterization Tester

PGY-SSM-EV-Tester is a AC/DC characterization platform provides flexibility to make AC/DC measurement of eMMC, SD and MicroSD devices at different operating modes enabling the validation engineers to do in-depth automated electrical and timing performance analysis to ascertain endurance and reliability of eMMC and SD devices. This test solution saves significant test time and reduces human errors.

PGY-SSM-EV-Tester eMMC and SD AC/DC Electrical Validation platform provides comprehensive electrical validation data to characterize eMMC devices for eMMC 4.41, 4.51, 5.0 and 5.1 (HS400) and SD 2.0/3.0 specifications. This innovative solution enables the validation engineers to run test cases to test different specifications and make all electrical parametric measurements. It covers 100s of measurements which could be completed in an hour instead of spending few days to complete them.



PGY-SSM-EV AC/DC Characterization platform



PGY-SSM-EV-Tester interfaces to host computer using USB3.0 interface. User can run standard test cases to test either eMMC and SD devices using software GUI. Product provides flexibility to write custom scripting the test cases to analyze the AC/DC performance to meet user need. PGY-SSM-EV-Tester S/W that runs in Host computer remotely controls oscilloscope to acquire current and voltage signals and analyses it for AC/DC electrical eMMC/SD parameters as per Specifications. PGY-SSM-EV-tester provides hooks to connect oscilloscope voltage and current probes and acquire voltage and current signals while running the test cases to make it convenient to use the test platform for AC/DC comprehensive Electrical characterization of eMMC and SD Devices.



 Measures AC/DC Electrical Measurements as per eMMC 4.41, 4.51, 5.0 and 5.1 Specification

- Measures AC/DC Electrical measurements as per SD2.0/3.0(UHS-I) Specification
- Standard test cases to make measurement at different data rate
- Flexibility to test the device for min and max limits of the specification
- Tolerance testing of devices outside the limits
- Statistical measurements to enhance the reliable of measurements
- Powerful debugging capabilities of AC/DC measurements in oscilloscope waveform
- Protocol Decoding of Command Signal and Data blocks of acquired with CRC check
- Upgradable to Protocol Analysis
- Flexibility to vary the clock, CMD and data signals timing parameters
- Supports API for full test automation
- Report Generation with test results
- Customized Test Reports





Oscilloscope setup view

PGY-SSM-EV-Tester eMMC/SD Electrical validation software captures the clock, command, and data signals. PGY-SSM-EV-Tester software running in host computer connects to oscilloscope using LAN interface. Optionally, user can also run this software inside Tektronix MSO6 series oscilloscope and make the analysis.



PGY-SSM-EV AC/DC measurement software

PGY-SSM-EV-Tester Software runs in host computer with windows OS. PGY-SSM EV software communicates with Tester hardware using USB interface and connects to Oscilloscope using LAN cable. User has flexibility to initialize SD or eMMC device and then run different test cases in different operating modes of SD or eMMC devices. PGY-SSM-EV software analyzes the oscilloscope acquired waveform for AC/DC parameter and displays the electrical measurements.

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	🔿 🗹 S01	104 1			^	Protocol	Decode Resu	ults —							1			
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	Clock P	eroid(tPERIOD)	4.8	NA	nS	SNo	Meas Name			Min	Mean	Max	Low Li	mit High Limit	Result	-	All Values	Result
	Output	Hold Time Response(tOH)	NA	NA	nS	1	Clock Freque	vcy		190.54 MI Iz	200.10 M	112 211.28	MHz 0.0000	12 208.00 MII		^ 1	3.9002 nS	0
	☑ Output	Hold Time Data Read(tOSU)	NA	NA	nS	2	Clock High Ti	me(tWH	0	1.4647 nS	1.8113 n	2.011	InS NA	NA	0	2	3.2133 nS	0
	2 Output	Delay Response(#0000)	NA	NA	105	3	Clock Low Tin	ne(tWL)		1.6614 nS	1.7575 ns	2.130	n5 NA	NA	0	3	3.9236 nS	0
1	2 August	Deles Date/ODI/O		1.01		4	Clock Rise Tin	ne(tTLH)	1	564.55 pS	717.34 pt	868.0	pS NA	960.00 pS	0	4	3.2488 nS	۲
1	(2) coupur	Delay Data(CDDC)	INA	INPA	ms	5	Clock Fall Tim	e((THL)		542.64 pS	714.43 ps	907.6	pS NA	960.00 pS	0	5	4.0666 nS	0
	☑ Output	Rising Time Response(tRISE)	NA	0.96	ns	6	Clock Duty C	rcle		44,427%	46.631%	48.85	% 30.000	% 70.000%	0	6	3.2816 nS	0
1	Output	Rising Time Data Read(tRISE)	NA	0.96	nS	7	Output Hold	Time Re	sponse((OII)	2.9855 nS	3.5400 n	4,128	nő NA	NΛ	0	7	4.0024 nS	0
1	🗹 Output	Falling Time Response(tFALL)	NA	0.95	nS	8	Output Rising	Time R	lesponse(tRIS	E) 400.50 pS	597.90 p3	755.5	pS NA	960.00 pS	0	8	3.4825 nS	0
	I Output	Falling Time Data Read(tFALL)	NA	0.96	ns	9	Output Falling	g Time F	Response(tFA)	LL) 539.21 pS	614.13 pt	698.4	pS NA	960.00 pS	0	9	3.9716 nS	0
	2 Output	Setup Time Response(tOSU)	NA	NA	nS	10	Input Hold TI	me(tiH)	Male and	911.24 pS	1.5015 ns	1.962	ins 800.01	ps NA		10	5.3576 hS	
	2 Output	Setun Time Data Read(COSLI)	NA	NA	15	12	Imput Field Ti	ine Data	a wrise(0H)	710 20 05	765 30 05	1.0500	10 600.01	950.00.05		11	3.4243 of	
4	Zour	1 Eak Maleran APA B	1.4	NIA.	10	13	Input Data Fa	ling Tin	ne	804.45 pS	1.0488 n	1.176	InS NA	960.00 pS	ő	13	3,7553 nS	ě
	- output	riigii suitage(sOH)	121	1505	v	14	Input Low Vol	Itagervi	u	196. mV	195. mV	195.0	W -300. m	V 580. mV		14	2.9855 nS	ě
	W Output	High Voltage(Voh Data Read)	1.4	NA	V	15	Input Low Vol	Itage(Vil	L Data Write)	21.4 mV	21.4 mV	21.4 n	-300. s	V 580. mV	0	15	3.7518 nS	0
	✓ Output	Low Voltage/VOI1	NA	0.45	V V	16	Instant Ulink 14	di man Ca	HIN .	1.670/	1 674	1.671/	1.1710	2.00V		14	2 2472	

PGY-SSM-EV software displays the electrical measurements with Pass/fail results with packet decode



List of Electrical parameters measured for eMMC card

concentra (The) </th <th>Measurements</th> <th>DS-BC</th> <th>HS-SDR</th> <th>HS-DDR</th> <th>HS-200</th> <th>HS-400</th>	Measurements	DS-BC	HS-SDR	HS-DDR	HS-200	HS-400
cock remefful)·/··/··/··/··/··/·Cack righ inversion·/··/	Clock Frequency	✓	√	1		
code time(th) </td <td>Clock Rise Time(tTLH)</td> <td>~</td> <td>✓</td> <td>1</td> <td>1</td> <td>1</td>	Clock Rise Time(tTLH)	~	✓	1	1	1
cocking/twith··· <t< td=""><td>Clock Fall Time(tTHL)</td><td>✓</td><td>1</td><td>1</td><td>1</td><td>1</td></t<>	Clock Fall Time(tTHL)	✓	1	1	1	1
clock bried(with)III <td>Clock High Time(tWH)</td> <td>✓</td> <td>✓</td> <td>1</td> <td></td> <td></td>	Clock High Time(tWH)	✓	✓	1		
Clock Dury CycleIIIIIIClock Dury CycleIII <tdi< td="">IIII<</tdi<>	Clock Low Time(tWL)	~	1	1		
Clock Period(PESDC)III<	Clock Duty Cycle	~	√	1	1	1
Output Low Voltage(VCI) Data Axed)IIIIIOutput Hising Inter Besponse(RSE)III	Clock Period(tPERIOD)	~	1	1	1	1
Output Low Valuage(VCH Data Read)IIIIICatput Haing Time Response(URSE)III <t< td=""><td>Output Low Voltage(VOL)</td><td>~</td><td>~</td><td>1</td><td>1</td><td>1</td></t<>	Output Low Voltage(VOL)	~	~	1	1	1
Dutp Hsing Time Response(HIRE)IIIIChipp Hsing Time Data Read(HIRE)IIIIIICutput Fail Time Response(FAL)II </td <td>Output Low Voltage(VOH Data Read)</td> <td>~</td> <td>~</td> <td>1</td> <td>1</td> <td>1</td>	Output Low Voltage(VOH Data Read)	~	~	1	1	1
Durput Hising Time Body Deckel (SHS)IIIIIOutput Eding Time Response(ISAL)II <tdi< td="">IIII</tdi<>	Output Rising Time Response(tRISE)	✓	√	1		
Output Failing Time Response(FALL)✓✓✓✓✓Output Failing Time Bota Read(FALL)✓✓✓ <td>Output Rising Time Data Read(tRISE)</td> <td>✓</td> <td>√</td> <td>1</td> <td></td> <td></td>	Output Rising Time Data Read(tRISE)	✓	√	1		
Output Failing Time Data Read(FALL)IIIIIOutput Delay Response(CONY)IIIIIOutput Delay Data(CONY)IIIIIOutput Delay Data(CONY)IIIIIIOutput Belay Time Response(CON)II	Output Falling Time Response(tFALL)	✓	√	1		
Dutput beiny back (DDLY)IIIIIOutput beiny back (DDLY)IIIIIOutput setup Time back seques (DSU)IIIIIOutput setup Time back seques (DSU)IIIIIOutput setup Time back seques (DSU)IIIIIIOutput Hold Time Bespense (DSU)III<	Output Falling Time Data Read(tFALL)	✓	1	1		
Dutput belay back (DOLY)IIIIIOutput Setup Time Response((DSU)IIIIIOutput Setup Time Response(ON)IIIIIOutput Halt Time Response(ON)IIIIIOutput Halt Time Data Read(IOSU)IIIIIIOutput Halt Time Data Read(IOSU)II<	Output Delay Response(tODLY)	✓	√	1		
Output Setup Time Beasense(IOSU)IIIIOutput Setup Time Data Bead(IOSU)IIIIIOutput Hold Time Beasense(IOH)IIIIIIOutput Hold Time Beasense(IOH)II<	Output Delay Data(tODLY)	✓	1	1		
Output Setup Time Data Read(IOSU)IIIIOutput Hold Time Response(IOH)IIIIIOutput Hold Time Response(IOH)IIIIIIOutput High Voltage(Voh)II	Output Setup Time Response(tOSU)	~	√	1		
Output Hold Time Response(tXH)IIIOutput Hold Time Data Read(tOSU)IIIIOutput High Valtage(VAH)IIIIIOutput High Valtage(VAH)IIIIIIInput Setup Time Command(tSU)IIIIIIIInput Setup Time Data Write(tRU)III <tdi< td="">IIII</tdi<>	Output Setup Time Data Read(tOSU)	~	1	1		
Output High Voltage(Voh)Image: Additional and the additional ad	Output Hold Time Response(tOH)	✓	√	1		
Output High Voltage(VOH)IIIIIOutput High Voltage(Voh Data Read)III	Output Hold Time Data Read(tOSU)	~	1	1		
Output High Voltage(Vch Data Read)✓✓✓✓✓Input Setup Time Command(ISU)✓✓✓✓✓✓Input Setup Time Cota Write(ISU)✓✓✓✓✓✓Input Hold Time Otat Write(ISU)✓✓✓✓✓✓Input Hold Time Data Write(ISH)✓✓✓✓✓✓Input Hold Time Data Write(ISH)✓✓✓✓✓✓Input Hold Time Data Write(ISH)✓✓✓✓✓✓Input Hold Data Write)✓✓✓✓✓✓✓Input High Voltage(VIL Data Write)✓✓✓<	Output High Voltage(VOH)	~	√	1	1	✓
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Input Hold Time(IH)Imput Hold Time Data Write(IH)Imput Hold Time Data WriteImput Hold Time Data Write)Imput Hold Time Data WriteImput Hold Time Data WriteImput Hold Time Data WriteImput Hold Time Data WriteImput Data Raing Time Data Writ	Input Setup Time Data Write(tISU)	✓	√	1	~	✓
Input Hold Time Data Write(tiH)✓✓✓✓✓Input Low Voltage(VIL)✓✓✓✓✓✓Input twy Voltage(VIL)✓✓✓✓✓✓Input High Voltage(VIH)✓✓✓✓✓✓Input High Voltage(VIH)✓✓✓✓✓✓Input High Voltage(VIH) Clock)✓✓✓✓✓✓Input Aligh Voltage(VIL Clock)✓✓✓✓✓✓Input Data Rising Time✓✓✓✓✓✓Input Data Rising Time✓✓✓✓✓✓Input Data Rising Time Data Write✓✓✓✓✓✓✓Input Data Rising Time Data Write✓✓✓	Input Hold Time(tIH)	✓	√	1	1	✓
Input Low Voltage(VIL)✓✓✓✓✓Input Low Voltage(VIL) Data Write)✓✓✓✓✓✓Input High Voltage(VIH)✓✓✓✓✓✓✓Input High Voltage(VIH) Data write)✓✓ </td <td>Input Hold Time Data Write(tIH)</td> <td>✓</td> <td>1</td> <td>1</td> <td>1</td> <td>✓</td>	Input Hold Time Data Write(tIH)	✓	1	1	1	✓
Input Low Voltage(ViL Data Write)Imput High Voltage(ViH)Imput High Voltage(ViH)Imput High Voltage(ViH)Imput High Voltage(ViH)Imput High Voltage(ViH Data write)Imput High Voltage(ViH Data write)Imput High Voltage(ViH Clock)Imput Data WriteImput Data Resign TimeImput Data Resign Time Data WriteImput Data Resign Time Data WriteImput Data Resign Time Data WriteImput Data Reling Time Data WriteImput Data Reling Time Data WriteImput Data Falling Time Data WriteImput Data Falling Time Data WriteImput Data Reling Time Data	Input Low Voltage(VIL)	✓	√	1	1	✓
Input High Voltage(VIH)VVVVInput High Voltage(VIH Clock)VVVVVInput High Voltage(VIH Clock)VVVVVInput Low Voltage(VIH Clock)VVVVVInput Data Rising TimeVVVVVInput Data Rising TimeVVVVVInput Data Rising Time Data WriteVVVVVInput Data Rising Time Data WriteVVVVVValid Window Response(tVW)VVVVVVValid Window Response(tVW)VVVVVVValid Window Data Read(tVH)VVVVVVOutput Delay Response(tPH)VVVVVVOutput Delay Data Read(tPH)VVVVVVDuty Cycle DistortionVVVVVVMinimum Pulse WidthVVVVVVMinimum Pulse Width ClockVVVVVStorbe Deriod(IPEROD)VVVVVOutput Skew Time(tRQ)VVVVV <td>Input Low Voltage(ViL Data Write)</td> <td>✓</td> <td>1</td> <td>1</td> <td>1</td> <td>✓</td>	Input Low Voltage(ViL Data Write)	✓	1	1	1	✓
Input High Voltage(ViH Data write)Imput High Voltage(ViH Clock)Imput High Voltage(ViH Clock)Imput High Voltage(VII Clock)Imput Data Rising TimeImput Data Rising TimeImput Data Rising TimeImput Data Rising Time Data WriteImput Data Falling Time Data WriteImput Data Radi(tww)Imput Data Radi(tww)Imput Data Read(tww)Imput Dat	Input High Voltage(VIH)	~	✓	1	1	✓
Input High Voltage(VIH Clock)✓✓✓✓✓Input Low Voltage(VIL Clock)✓✓✓✓✓Input Data Rising Time✓✓✓✓✓Input Data Rising Time Data Write✓✓✓✓✓Input Data Falling Time Data Write✓✓✓✓✓Input Data Falling Time Data Write✓✓✓✓✓Input Data Falling Time Data Write✓✓✓✓✓Valid Window Response(tVW)✓✓✓✓✓Valid Window Data Read(tVW)✓✓✓✓✓Output Delay Reagnes(tPH)✓✓✓✓✓Output Delay Read(tPH)✓✓✓✓✓Duty Cycle Distortion✓✓✓✓✓Minimum Pulse Width✓✓✓✓✓Minimum Pulse Width Clock✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓ <t< td=""><td>Input High Voltage(ViH Data write)</td><td>✓</td><td>√</td><td>1</td><td>1</td><td>✓</td></t<>	Input High Voltage(ViH Data write)	✓	√	1	1	✓
Input Low Voltage(VIL Clock)✓✓✓✓Input Data Rising Time✓✓✓✓Input Data Rising Time Data Write✓✓✓✓Input Data Rising Time Data Write✓✓✓✓Input Data Falling Time Data Write✓✓✓✓Input Data Falling Time Data Write✓✓✓✓Input Data Falling Time Data Write✓✓✓✓Valid Window Response(tVW)✓✓✓✓Valid Window Data Read(tVW)✓✓✓✓Output Delay Response(tPH)✓✓✓✓Output Delay Read Read(tPH)✓✓✓✓Duty Cycle Distortion✓✓✓✓Minimum Pulse Width✓✓✓✓Minimum Pulse Width Clock✓✓✓✓Slew Rate✓✓✓✓Output Hold Skew Time(tRQ)✓✓✓✓Strobe Period(tPERIOD)✓✓✓✓	Input High Voltage(VIH Clock)	√	1	1	1	✓
Input Data Rising TimeImput Data Rising Time Data WriteImput Data Rising Time Data WriteImput Data Raing Time Data WriteImput Data Falling Time Data Fall	Input Low Voltage(VIL Clock)	√	1	1	1	1
Input Data Rising Time Data WriteImage: Constraint of the c	Input Data Rising Time			1		
Input Data Falling TimeImput Data Falling Time Data WriteImput Data Falling T	Input Data Rising Time Data Write		1	1		
Input Data Falling Time Data WriteImput Data Falling Time Data Read(tPM)Imput Data Read(tPM)Imput Data Read(tPM)Imput Data Falling Time Data Read(tPM)Imput Data Read(tPM)Im	Input Data Falling Time		1	1		
Valid Window Response(tVW)Image: Constraint of the second sec	Input Data Falling Time Data Write		1	1		
Valid Window Data Read(tVW)Image: Constraint of the second se	Valid Window Response(tVW)				1	
Output Delay Response(tPH)Image: Constraint of the system of	Valid Window Data Read(tVW)				1	
Output Delay Data Read(tPH)Image: Constraint of the second se	Output Delay Response(tPH)				1	
Duty Cycle DistortionImage: Constraint of the second s	Output Delay Data Read(tPH)				1	
Strobe Duty Cycle DistortionImage: Constraint of the stress o	Duty Cycle Distortion					✓
Minimum Pulse WidthMinimum Pulse Width ClockImage: Clock of the state of th	Strobe Duty Cycle Distortion					1
Minimum Pulse Width ClockImage: Constraint of the sector of t	Minimum Pulse Width					✓
Slew RateImage: Slew RateImage: Slew RateOutput Hold Skew Time(tRQH)Image: Slew RateImage: Slew RateOutput Skew Time(tRQ)Image: Slew RateImage: Slew RateStrobe Period(tPERIOD)Image: Slew RateImage: Slew Rate	Minimum Pulse Width Clock					1
Output Hold Skew Time(tRQH)Image: Constraint of the second se	Slew Rate					✓
Output Skew Time(tRQ) Image: Constraint of the constra	Output Hold Skew Time(tRQH)					✓ ✓
Strobe Period(tPERIOD)	Output Skew Time(tRQ)					√
	Strobe Period(tPERIOD)					√
Output Skew Time(tRQ_CMD)	Output Skew Time(tRQ_CMD)					✓ ✓
Output Hold Skew Time(tRQH_CMD)	Output Hold Skew Time(tRQH_CMD)					1





Measurements	Default speed	Hlgh Speed	SDR12	SDR25	SDR50	DDR50	SDR104
Clock Frequency	1	1	1	1	1	1	1
Clock Rise Time(tTLH)	1	1	1	1	1	1	1
Clock Fall Time(tTHL)	1	1	1	1	1	1	1
Clock High Time(tWH)	1	1	1	1	1	1	1
Clock Low Time(tWL)	1	1	1	1	1	1	1
Clock Duty Cycle	1	1	1	1	1	1	1
Clock Period(tPERIOD)	1	1	1	1	1	1	1
Output Low Voltage(VOL)	1	1	1	1	1	1	1
Output Low Voltage(VOH Data Read)	1	1	1	1	1		1
Output Rising Time Response(tRISE)			1	1	1	1	1
Output Rising Time Data Read(tRISE)			1	1	1		1
Output Falling Time Response(tFALL)			1	1	1	1	1
Output Falling Time Data Read(tFALL)			1	1	1		1
Output Delay Response(tODLY)			1	1	1	1	1
Output Delay Data(tODLY)	1	1	1	1	1	1	1
Output Setup Time Response(tOSU)			1	1	1	1	1
Output Setup Time Data Read(tOSU)			1	1	1		1
Output Hold Time Response(tOH)		1	1	1	1	1	1
Output Hold Time Data Read(tOSU)		1	1	1	1		1
Output High Voltage(VOH)	1	1	1	1	1	1	1
Output High Voltage(Voh Data Read)	1	1	1	1	1		1
Input Setup Time Command(tISU)	1	1	1	1	1	1	1
Input Setup Time Data Write(tISU)	1	1	1	1	1		1
Input Hold Time(tIH)	1	1	1	1	1	1	1
Input Hold Time Data Write(tIH)	1	1		1	1		1
Input Low Voltage(VIL)	1	1	1	1	1	1	1
Input Low Voltage(ViL Data Write)	1	1	1	1	1		1
Input High Voltage(VIH)	1	1	1	1	1	1	1
Input High Voltage(ViH Data write)	1	1	1	1	1		1
Input High Voltage(VIH Clock)	1	1	1	1	1	1	1
Input Low Voltage(VIL Clock)	1	1	1	1	1	1	1
Input Data Rising Time			1	1	1	1	1
Input Data Rising Time Data Write			1	1	1		1
Input Data Falling Time			1	1	1	1	1
Input Data Falling Time Data Write			1	1	1		1
Output Delay Response(tPH)	1						
Clock Cycle Time			1				
Card Output Phase Response(top)							1
Card Output Phase Data Read(top)							1
Output Data Window Response(Todw)							1
Output Data Window Data Read(Todw)							1





Ordering Information

PGY-SSM-EV-Tester SD and eMMC AC/DC Electrical Characterization Tester. *(Shipment includes Hardware, software CD)*

Prerequisite Tektronix MSO5/6 oscilloscope series with passive probes.

Warranty Information

• Hardware and software carries warranty of one year.



About Prodigy Technovations Pvt Ltd

Prodigy Technovations is the leading provider of innovative protocol analysis solutions for mainstream and emerging technologies. We provide Protocol Decode, and PHY layer testing solutions on Test & Measurements equipment's. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol Analysis solutions using latest hardware technologies.