

## PGY-UFS3.X-PA MPHY, UniPro, UFS Protocol Analyzer



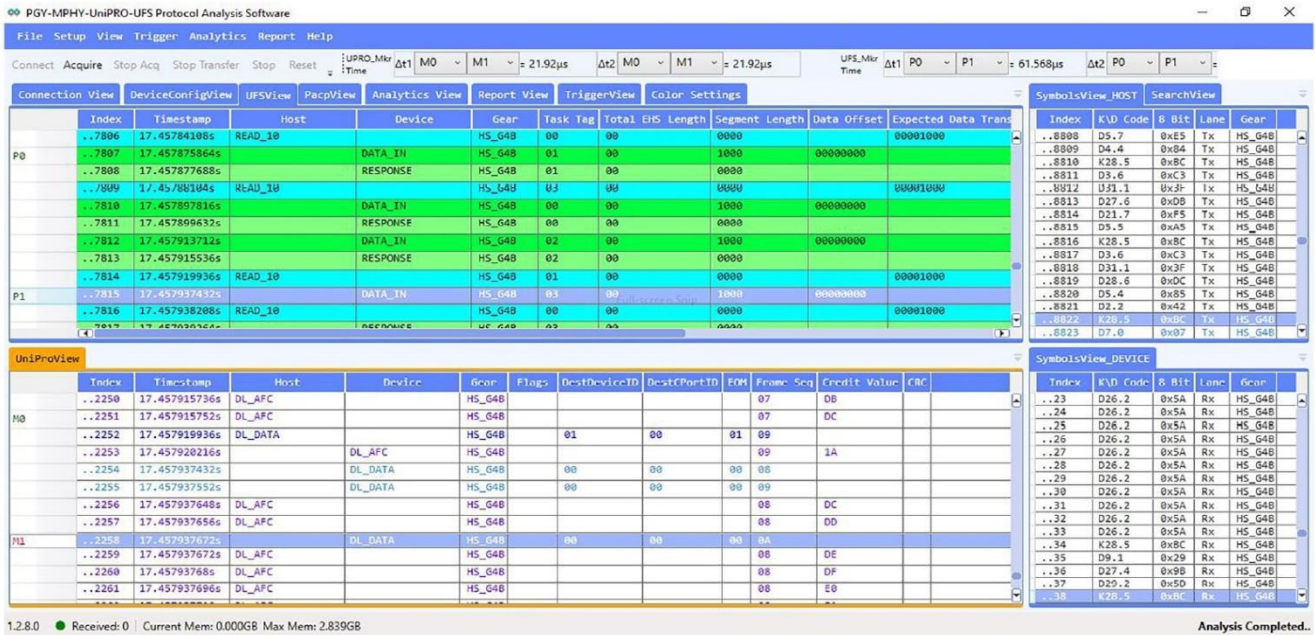
UFS Protocol Analyzer(PGY-UFS3.X-PA) is the Protocol Analyzer with multiple features to capture and debug communication between host and design under test. PGY-UFS3.X-PA, UFS Protocol Analyzer, a value-based analyzer in its class, offers capture and debugging of data across MPHY, UniPro, and UFS protocol layers. It allows for instantaneous decoding of the UFS layer, UniPro layer, and MPHY layer with the flexibility to correlate decoded data across these protocol layers.

PGY-UFS3.X-PA supports PWMG1 to HSG4B data rates and two TX, and two RX lane decode. The active probe has minimum electrical loading on the device under test (DUT) and captures protocol data without affecting the performance of DUT. PGY-UFS3.X-PA Protocol Analyzer supports two-lane data. Comprehensive decoding of UniPro & UFS data on the Fly enables validation of communication between UFS host and device.

PGY-UFS3.X-PA Protocol Analyzer allows Design and Test Engineers to obtain deep insight into UFS host and device communication. MPHY/UniPRO/UFS packet-based triggering allows specific protocol data capture and analysis. PGY-UFS Protocol analyzer instantaneously provides decoding of UFS, UniPro, and MPHY layers with a correlation to MPHY, UniPro, and UFS layers.

Solder down active probes allows probing of the MPHY test points. This allows the design and test engineers to capture UFS traffic between the host and UFS memory with high signal fidelity. Today's test engineers need to test the use case scenarios in their labs that mimic real-life use cases. The PGY-UFS3.X-PA, UFS Protocol Analyzer has been designed to enable engineers to closely monitor and analyze the traffic between the host and the device while executing the various use case scenarios.

Windows-based protocol analysis software provides the industry's best protocol correlation between UFS to UniPro and MPHY layers. Time correlation between the different protocol layers significantly reduces debug time of designs. The floating window design of this software allows engineers to view the UFS view, UniPro view, and MPHY view on different computer monitors and automatically correlate the UFS packets to the MPHY layer. This makes analysis very easy while analyzing the gigabytes of Protocol information.



The screenshot displays the PGY-MPHY-UniPro-UFS Protocol Analysis Software interface. The main window is divided into several panes:

- Top Panel:** Includes menu options (File, Setup, View, Trigger, Analytics, Report, Help) and control buttons (Connect, Acquire, Stop Acq, Stop Transfer, Stop, Reset). It also shows configuration for UFS\_Mkr Time, Δt1, Δt2, UFS\_Mkr Time, Δt1, P0, P1, and Δt2, P0, P1.
- Connection View:** Shows a table with columns: Index, Timestamp, Host, Device, Gear, Task Tag, Total EHS Length, Segment Length, Data Offset, and Expected Data Trans.
- UniProView:** Shows a table with columns: Index, Timestamp, Host, Device, Gear, Flags, DestDeviceID, DestPartID, FRM, Frame Seq, Credit Value, and CRC.
- SymbolsView\_HOST and SymbolsView\_DEVICE:** Show detailed symbol information with columns: Index, K/D Code, 8 Bit, Lane, Gear.

At the bottom, the status bar indicates: 1.2.8.0 Received: 0 Current Mem: 0.000GB Max Mem: 2.839GB Analysis Completed.

## Key Features

- ✦ Supports version MPHY 4.0, UniPro 1.8, and UFS version 2.1/3.1.
- ✦ Supports PWM G1 to G7 and HS G1,2,3,4 A and B Series · Supports one/two data lanes (2 TX and 2 RX).
- ✦ Flexibility to capture very large data using continuous streaming of Protocol data to host computer.
- ✦ Hardware-based circular buffer.
- ✦ Flexibility to decode selected data from 8GB Buffer.
- ✦ Solder down active probe provides high signal fidelity.
- ✦ Decoding at MPHY, UniPro, and UFS layer.
- ✦ Trigger-based on MPHY, UniPro, UFS layer packet content.
- ✦ Supports triggering in PWM and HS data rate speeds.
- ✦ Trigger out a signal at the trigger event allows the triggering of other instruments such as oscilloscope.
- ✦ Interface to host system using USB3.0 or Gigabit Ethernet Interface.
- ✦ Flexibility to upgrade the hardware firmware using the GbE interface provides easy field up-gradation of FPGA firmware.
- ✦ Decoded data packets can be exported to a text file for further analysis.
- ✦ PGY-UFS3.0-PA Protocol Analyzer is lightweight and can be deployed for on-site/ field tests.

## Test Setup



PGY-UFS3.X-PA UFS Protocol Analyzer provides USB3.0 and Gbe interface for host computer connectivity. High-speed host connectivity enables continuous streaming of protocol data to host HDD and storage for a long period of time. The software offers multi-view such as MPHY view, UniPro view, and UFS View. Each view lists the respective protocol packets and their details with a correlation of each layer for easy debugging. The lightweight Analyzer is easy to carry during a field visits.

## Equalizer and Memory

**Advanced Settings**

<p><b>Burst Speed Detection</b></p> <p><input type="radio"/> Sync Speed</p> <p><input checked="" type="radio"/> PACP PWR Gear</p>	<p><b>Sync Wait Time</b></p> <p>Host <input type="text" value="10"/></p> <p>Device <input type="text" value="32"/></p>	<p><b>Host</b></p> <p>CTLE <input type="text" value="MANUAL"/></p> <p>DFE Gain <input type="text" value="MANUAL"/></p> <p>Freq Boost <input type="text" value="5"/></p> <p>Wide Band Gain <input type="text" value="7"/></p> <p>DFEGain CFG <input type="text" value="31"/></p>	<p><b>Device</b></p> <p>CTLE <input type="text" value="MANUAL"/></p> <p>DFE Gain <input type="text" value="MANUAL"/></p> <p>Freq Boost <input type="text" value="0"/></p> <p>Wide Band Gain <input type="text" value="0"/></p> <p>DFEGain CFG <input type="text" value="31"/></p>
---	--	---	---

**Acquisition/Error Analysis**

<p><b>Analyze</b></p> <p><input type="radio"/> Live Decode</p> <p><input checked="" type="radio"/> Post Capture</p>	<p><b>Hardware Filters</b></p> <p><input checked="" type="checkbox"/> AFC</p> <p><input type="checkbox"/> DLData Payload Drop</p>	<p><b>Buffer Type</b></p> <p><input checked="" type="radio"/> Continuous/8GB</p> <p><input type="radio"/> Circular (H/W)</p> <p>Buffer Size <input type="text" value="100"/> MB</p> <p>PreTrigger <input type="text" value="0"/> MB</p>	<p><b>CRC Error Count</b></p> <p><input type="checkbox"/> DLData</p> <p><input type="checkbox"/> AFC</p>
---	---	---	--

PGY-UFS3.X provides the flexibility to the set TX and RX CTLE and DFE equalizer to address reflection and poor SI signals while probing the MPHY signals. This helps in reducing the error decoding of packets. A newly introduced hardware-based circular buffer provides the flexibility to continuously capture the protocol data and analyze the data in circular buffer size. Users can set triggers on the circular buffer and capture the protocol data at specific events.



## UFS Protocol Layer Decode

Index	Timestamp	Host	Device	Gear	Task Tag	Total BPS Length	Segment Length	Data Offset	Expected D	Logical Block Adc	Device In	Transfer Le	Response
..7809	17.45788104s	READ_10		HS_G4B	03	00	0000		00001000	005E2886		0001	
..7810	17.457897816s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7811	17.457899632s		RESPONSE	HS_G4B	00	00	0000				00		Success (00)
..7812	17.457913712s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7813	17.457915536s		RESPONSE	HS_G4B	02	00	0000				00		Success (00)
..7814	17.457919936s	READ_10		HS_G4B	01	00	0000		00001000	005E5B72		0001	
..7815	17.457937432s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7816	17.457938208s	READ_10		HS_G4B	00	00	0000		00001000	005DDF2E		0001	
..7817	17.457939264s		RESPONSE	HS_G4B	03	00	0000				00		Success (00)
..7818	17.457974088s	READ_10		HS_G4B	02	00	0000		00001000	005E707A		0001	
..7819	17.457975048s		DATA_IN	HS_G4B	01	00	1000	00000000					
..7820	17.457980872s		RESPONSE	HS_G4B	01	00	0000				00		Success (00)
..7821	17.457981648s	READ_10		HS_G4B	03	00	0000		00001000	005E2517		0001	
..7822	17.457994904s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7823	17.457996808s		RESPONSE	HS_G4B	00	00	0000				00		Success (00)
..7824	17.458019368s	READ_10		HS_G4B	01	00	0000		00001000	005E5B7C		0001	
..7825	17.458031576s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7826	17.458031672s	READ_10		HS_G4B	00	00	0000		00001000	005DAD56		0001	
..7827	17.4580334s		RESPONSE	HS_G4B	02	00	0000				00		Success (00)
..7828	17.458037632s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7829	17.458039448s		RESPONSE	HS_G4B	03	00	0000				00		Success (00)
..7830	17.458073704s	READ_10		HS_G4B	02	00	0000		00001000	005E8D79		0001	
..7831	17.458076264s		DATA_IN	HS_G4B	01	00	1000	00000000					
..7832	17.458078088s		RESPONSE	HS_G4B	01	00	0000				00		Success (00)
..7833	17.458083496s	READ_10		HS_G4B	03	00	0000		00001000	005E0192		0001	
..7834	17.458087656s		DATA_IN	HS_G4B	00	00	1000	00000000					
..7835	17.45808948s		RESPONSE	HS_G4B	00	00	0000				00		Success (00)
..7836	17.458116096s	READ_10		HS_G4B	01	00	0000		00001000	005E52A4		0001	
..7837	17.45812792s	READ_10		HS_G4B	00	00	0000		00001000	005D8026		0001	
..7838	17.4581308s		DATA_IN	HS_G4B	02	00	1000	00000000					
..7839	17.458132224s		RESPONSE	HS_G4B	02	00	0000				00		Success (00)
..7840	17.458140168s		DATA_IN	HS_G4B	03	00	1000	00000000					
..7841	17.458141992s		RESPONSE	HS_G4B	03	00	0000				00		Success (00)
..7842	17.458170272s	READ_10		HS_G4B	02	00	0000		00001000	005E7F40		0001	

PGY-UFS3.X-PA Software can display each UFS packet parameter in a listing window. Right-click lists all the packet parameters for user selection. Users can color code the fonts or background color for easy identification of each UFS packet.

## PACP and UniPro View

PGY-MPHY-UniPRO-UFS Protocol Analysis Software

File Setup View Trigger Analytics Report Help

Connect Acquire Stop Acq Stop Transfer Stop Reset UFS\_Mkr Time Δt1 MO M1 21.92μs Δt2 MO M1 21.92μs UFS\_Mkr Time Δt1 PO P1 61.560μs Δt2 PO P1

Connection View DeviceConfigView UFSView PacpView Analytics View Report View TriggerView Color Settings SymbolsView\_HOST SearchView

Index	Timestamp	Direction	Description	Gear	Tx Gear	Tx Lane	Tx Mode	Rx Gear	Rx Lane	Rx Mode	Flags	CRC	MIBAttribute	MIBValue	LineReset
18	14.904759368s	H → D	PACP_PiR_req	HS_G1B	01	02	03	01	02	03	00				00
19	14.904763112s	H ← D	PACP_PiR_cnf	HS_G1B	01	02	03	01	02	03	00				00
20	14.9067222s	H → D	PACP_get_req	HS_G1B								009F			
21	14.906920152s	H ← D	PACP_get_cnf	HS_G1B								0000007F			
22	14.907325288s	H → D	PACP_PiR_req	HS_G1B	04	02	01	04	02	01	10				00
23	14.907329088s	H ← D	PACP_PiR_cnf	HS_G1B	04	02	01	04	02	01	10				00
24	14.957373936s	H → D	PACP_PiR_req	HS_G4B	04	02	03	04	02	03	00				00
25	14.957374264s	H ← D	PACP_PiR_cnf	HS_G4B	04	02	03	04	02	03	00				00
26	14.958731352s	H → D	PACP_PiR_req	HS_G4B	04	02	03	04	02	03	00				00
27	14.958731672s	H ← D	PACP_PiR_cnf	HS_G4B	04	02	03	04	02	03	00				00
28	15.082728184s	H → D	PACP_PiR_req	HS_G4B	04	02	03	04	02	03	00				00
29	15.082728464s	H ← D	PACP_PiR_cnf	HS_G4B	04	02	03	04	02	03	00				00
30	15.186224752s	H → D	PACP_PiR_req	HS_G4B	04	02	03	04	02	03	00				00

UniProView

Index	Timestamp	Host	Device	Gear	Flags	EDM	Frame Seq	Credit Value	CRC
..5766	14.95773084s		DL_AFC	HS_G4B			03	38	
..5767	14.958731352s		PACP_PiR_req	HS_G4B	00				
..5768	14.958731672s		PACP_PiR_cnf	HS_G4B	00				
..5769	14.95873184s		EDM	HS_G4B					
..5770	14.958732144s		EDM	HS_G4B					
..5771	14.976042456s		S0B	HS_G3B					
..5772	15.010263416s		S0B	HS_G4B					
..5773	15.010263416s		DL_AFC	HS_G4B		1F	00		
..5774	15.010263416s		DL_AFC	HS_G4B		1F	80		
..5775	15.010263768s		S0B	HS_G4B					
..5776	15.010263768s		DL_AFC	HS_G4B		1F	00		
..5777	15.010263768s		DL_AFC	HS_G4B		1F	34		

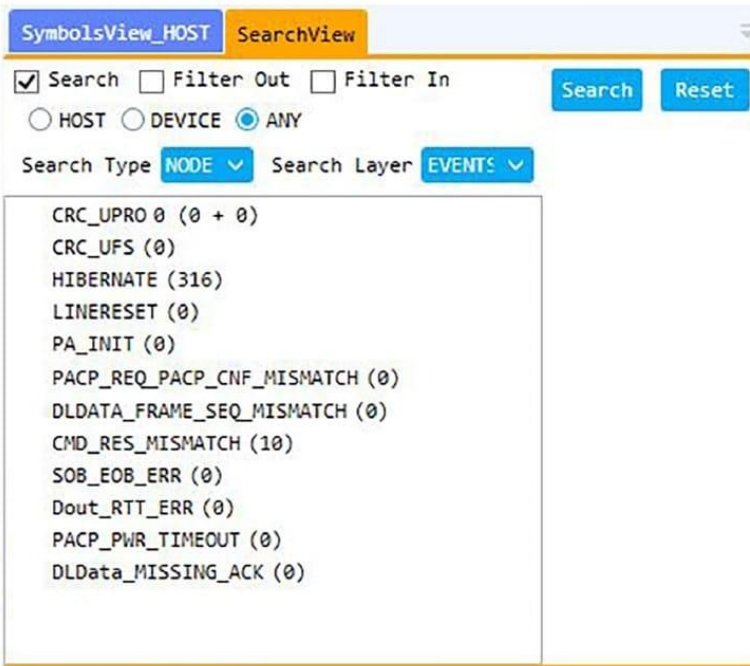
SymbolsView\_DEVICE

Index	KVD Code	8 Bit	Lane	Gear
..23	D26.2	0x5A	Rx	HS_G4B
..24	D26.2	0x5A	Rx	HS_G4B
..25	D26.2	0x5A	Rx	HS_G4B
..26	D26.2	0x5A	Rx	HS_G4B
..27	D26.2	0x5A	Rx	HS_G4B
..28	D26.2	0x5A	Rx	HS_G4B
..29	D26.2	0x5A	Rx	HS_G4B
..30	D26.2	0x5A	Rx	HS_G4B
..31	D26.2	0x5A	Rx	HS_G4B
..32	D26.2	0x5A	Rx	HS_G4B
..33	D26.2	0x5A	Rx	HS_G4B
..34	K28.5	0x8C	Rx	HS_G4B
..35	D9.1	0x29	Rx	HS_G4B
..36	D27.4	0x9B	Rx	HS_G4B
..37	D29.2	0x50	Rx	HS_G4B
..38	K28.5	0x8C	Rx	HS_G4B

12.8.0 Received: 0 | Current Mem: 0.000GB Max Mem: 2.839GB Analysis Completed..

PGY-UFS3.X-PA Software separates the PACP packets in a separate view for easy analysis of power mode change packets and links to UniPro packets. Users can view the MPHY states stall, prepare, and sync information in UniPro view apart from the user selection for L\_Data and AFC/NACK Packet details.

## Error Events, Search, and Filter



PGY-UFS3.X-PA Software does the live decode and lists all the events. The list of events is shown in this picture. Users can easily note the errors in captured protocol data. In large buffer capture, it takes extremely difficult to locate the errors. But PGY-UFS3.X-PA software simplifies this by listing events while decoding the captured data.

Search and Filter allows you directly locate the error events or UFS or UniPro or PACP packet in the protocol listing windows. Filter-in and Filter-out make it easy to view the data of interest in the protocol listing window.

## Comprehensive Protocol Analysis Using Multi-View

PGY-UFS3.X-PA UFS Protocol Analyzer provides USB 3.0 and Gbe interface for host computer connectivity. High-speed host connectivity enables continuous streaming of protocol data to host HDD and storage for a long period of time. The software offers multi-view such as MPHY view, UniPro view, and UFS View. Each view lists the respective protocol packets and their details with a correlation of each layer for easy debugging.





PGY Protocol Analyzer’s easy-to-use interface reduces the protocol analysis time. Time-stamped view of protocol decode listing provides an easy view of protocol activities between the host and the device. At a click of a button, the user can view the decode of each packet and the intended function. Floating window software architecture allows the user to view each protocol layer on separate monitors for easy debugging. Autocorrelation of each selected packet from UFS to MPHY layers simplifies the debug activity

## Specifications

Data Rates Supported	PWM G1 to G7, High Speed Gear 1, Gear 2, Gear 3 and Gear 4, Rate A and B
Link width	Configurable for 1TX/1RX or 2TX/2RX
Probes	Solder Down Active Probes
Protocol Decode	MPHY, UniPro and UFS layers
Trace Capture Size	Supports Continuous streaming of Protocol data to Host computer SSD/HDD. Tested for 30GB of Trace depth
Trigger	Based MPHY, UniPro, UFS Packets
Front Panel Connectors	Interface for Active probes. Trigger in/out SMA connectors
Interface for Host Computer	USB3.0 and Gigabit Ethernet interface
Host Computer Requirements	Windows 7/8.0/8.1/10 64bit operating System. It supports a RAM of minimum 8GB but the product would give a faster response for a 16GB. The minimum storage capacity of 1GB should be available in the hard disk drive. User can use more storage based on trace storage requirement. Display resolution of the monitor is 1024X768. Host computer should support USB3.0 or GBe interface.
Dimension	(W x H x D) (20.5X5X25) cms
Weight	Approx. 2.5Kg
Power Requirement	12V, 3A DC Power Supply (AC/DC Supplied along with Analyzer)



## Trigger specifications

Stack	Protocol Analyzer	Packet Type
	Link Start-up Sequence	(TRG_UPRO0)
		(TRG_UPRO1)
		(TRG_UPRO2)
UniPRO	PHY Capability Adapter Packets (PCAP)	PACP_PWR_reg
		PACP_PWR_cnf
		PAC_Cap_ind
		PACP_Cap_EXT1_ind
		PACO_EPR_ind
		PACP_TestMode_req
		PACP_GET_req
		PACP_GET_cnf
		PACP_SER_req
		PACP_SET_cnf
		PACP_TEST_Data_0
		PACP_TEST_Data_1
		PACP_TEST_Data_2
PACP_TEST_Data_3		
	Data Link Packets	SOF
		EOF
		EOF_ODD
		EOF_EVEN
		COF
		AFC/NAC
		Traffic class 0/Traffic class 1
UFS	UFS Layers Packets	NOP IN
		NOP OUT
		Commands
		Response
		Task Management Request
		Task Management Response
		Ready To Transfer
		Ready to Transfer



## Solder Down Probe Tips



P5021-L-WE 14 Gbps probe tips with passive equalizer at input



P5021-L 14 Gbps probe tip with isolation resistor



P5021 14 Gbps probe tips for direct access to test points

Probing the UFS signal is one of the key challenges in reliable UFS protocol decode. In most of the DUT, test points are located close to each other without enough space to solder the probe tips. Prodigy Technovations offers three types of 14 Gbps Probe tips which provide flexibility to choose the probe tips to meet the need. P5021-L and P5021-L-WE Probe tips have isolation resistors that can be changed based on the signal strength at test points. This helps in reducing reflections while accessing the test point and maintaining the signal integrity. The passive equalizer in P5021-L-WE helps in maintaining the differential impedance between the lane. If test points are easily accessible, then the P5021 probe tip can be used to probe the test points.

## Ordering Information

PGY-UFS3.X-PA UFS Protocol Analyzer

(Shipment includes Hardware, software CD, One set probe, USB3.0, Ethernet Cable and Power adapter)

## Warranty Information

Hardware and software carry a warranty of one year.

Probes are covered three-month warranty for any manufacturing defects





## Contact Information



+91-80-42126100



[contact@prodigytechno.com](mailto:contact@prodigytechno.com)



[www.prodigytechno.com](http://www.prodigytechno.com)



### **Prodigy Technovations Pvt. Ltd.**

294, 3rd Floor, 7th Cross,  
7th Main BTM II Stage,  
Bangalore 560076.  
Karnataka, India.

---

## About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd ([www.prodigytechno.com](http://www.prodigytechno.com)) is a leading global technology provider of Protocol Decode and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include the successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.