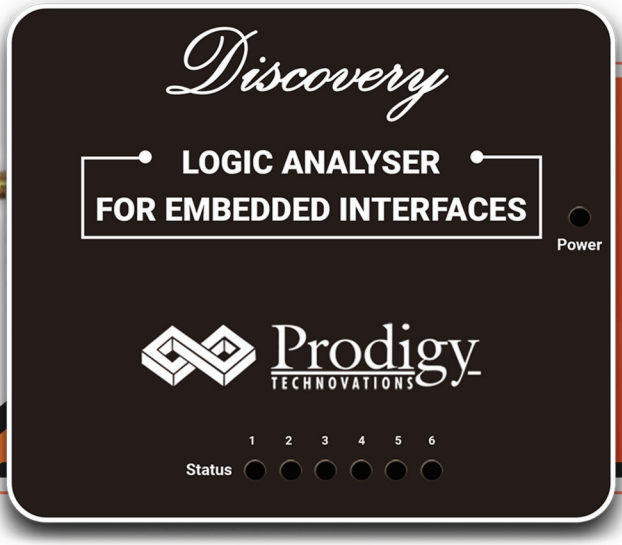
Logic Analyzer For Embedded Interfaces



The DISCOVERY series PGY-LA-EMBD logic analyzer with protocol decode capabilities is designed to debug the logic and protocol issues faced by embedded design teams in consumer, industrial, home automation, health and education sectors.

PGY-LA-EMBD is an industry first logic analyzer in its category which enables engineers to debug timing problems and perform simultaneous protocol analysis of I2C, SPI and UART interfaces in embedded designs. This enables designers debug circuit level and system level problems quickly.

PGY-LA-EMBD offers 1GS/Sec asynchronous (timing) data and 100Mhz synchronous (state) data capture which makes it an ideal debug tool to address the digital design problems. Designers can now easily analyze setup and hold time issues, glitches and synchronous data activities apart from analyzing protocol issues.

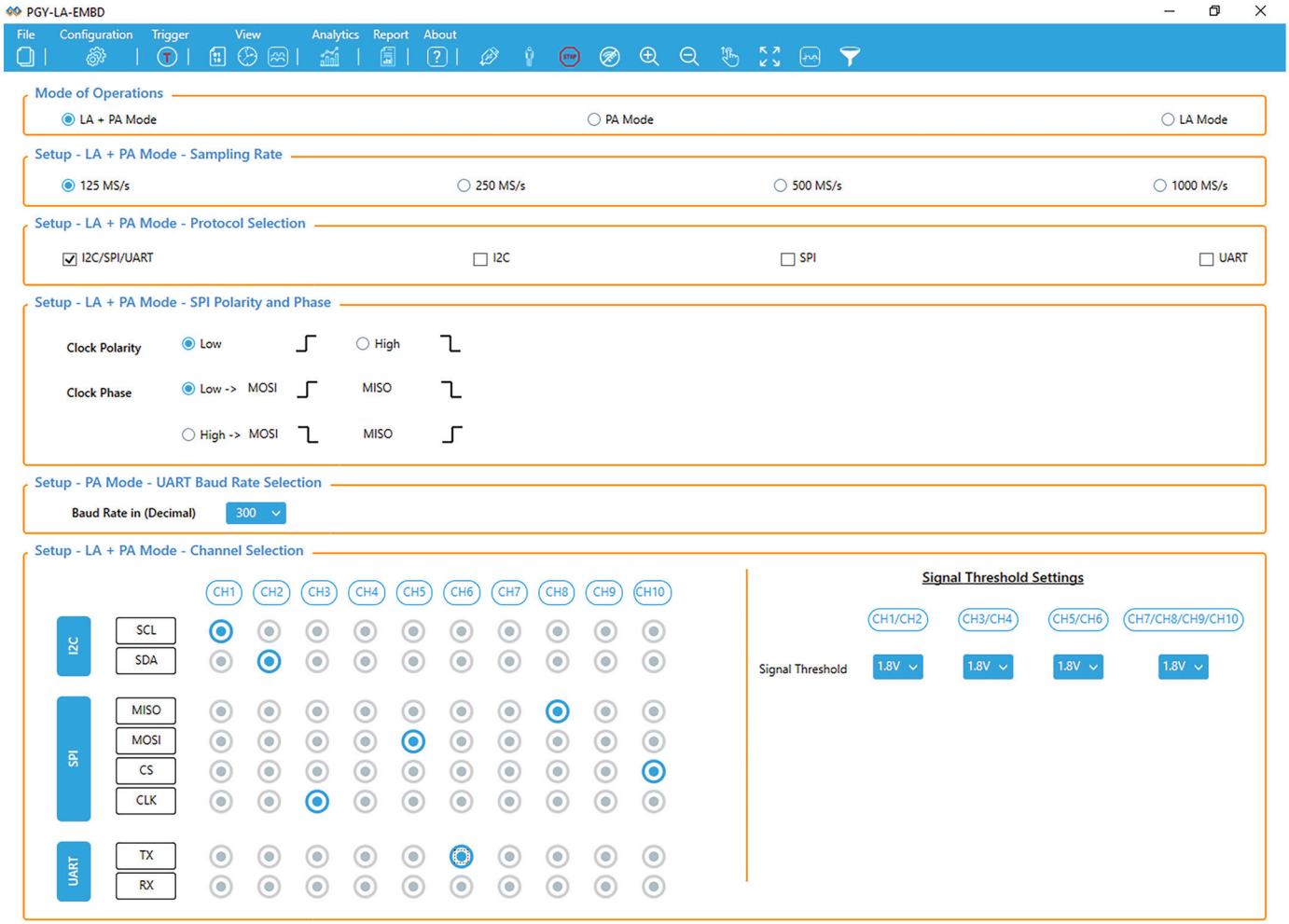
Current generation embedded designers need to collect data from multiple interfaces such as I2C, SPI and UART and process it to achieve optimal performance of their designs. Embedded design teams need to take timely action to meet the intended objectives of the product. PGY-LA-EMBD simultaneously decodes I2C, SPI and UART bus and displays the protocol activity with time stamp information. PGY-LA-EMBD is an ideal instrument to debug the hardware and embedded software integration issues and optimize the software performance.

Multiple markers enable smart delta measurements which are key to designers. Zoom enables users to look at specific areas of the signal.

Features

- 10 channels with Protocol and Logic Analysis capability
- 1GS/Sec Timing (Asynchronous) Analysis
- 100MHz State (Synchronous) Analysis
- Simultaneous Protocol Analysis of UART, SPI and I2C.
- Detailed Trigger capabilities: Auto, Pattern, Protocol aware (UART, SPI and I2C) and timing (pulse width and delay)
- Smart streaming of data from Protocol
- Analyzer to host computer for long duration capture using USB3 interface.
- Innovative easy to use Graphical user interface.
- Error Analysis of Protocol packet
- Provides timing, waveform, listing and Protocol listing views
- Detailed filtering capability for protocol decoded data
- PDF and CSV report format.
- API support.

Easy Configuration



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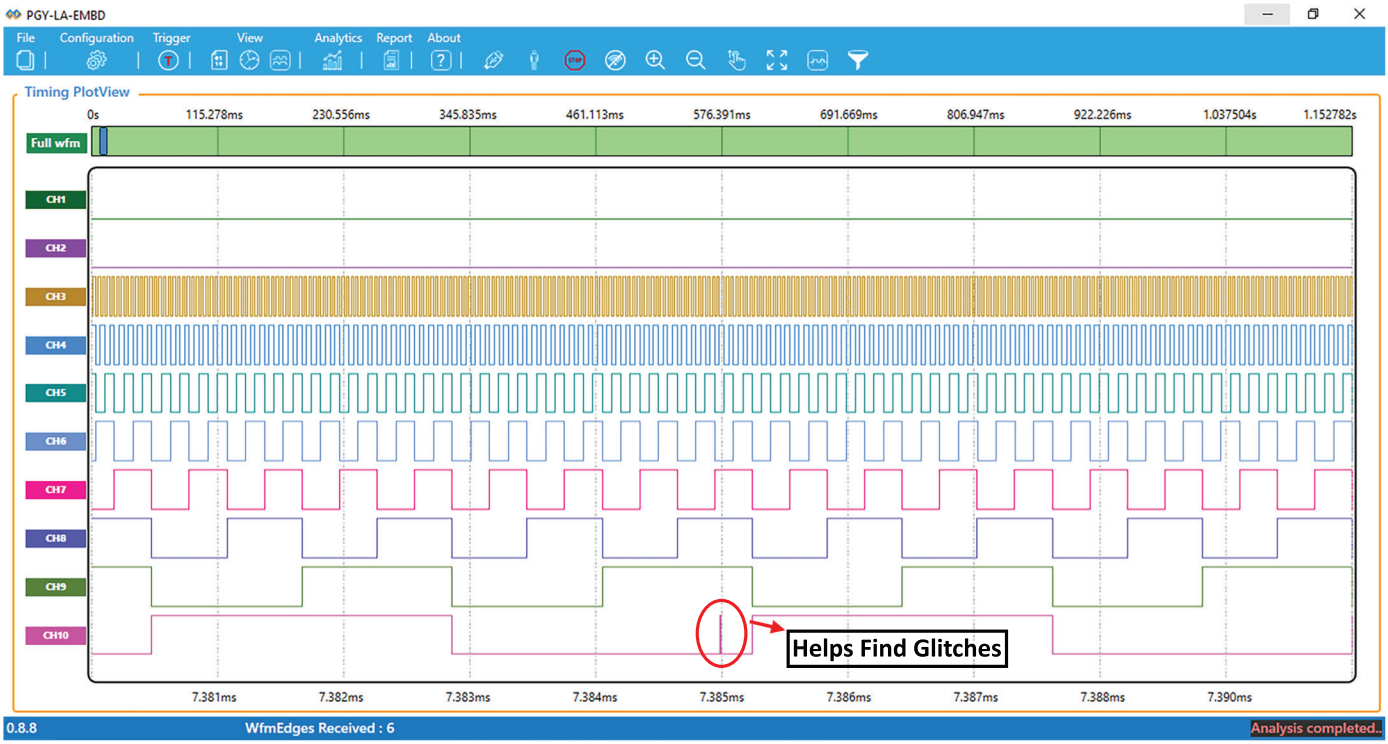
Users can easily configure the Logic Analyzer for embedded interfaces by either selecting Logic Analysis (LA) mode or Protocol Analysis (PA) mode or a combined (LA+PA) mode. This ensures a quick and easy way to configure the product and look at complex problems at system level either in Logic Analysis (State Analysis, Timing Analysis) or Protocol decoding or both. Save and Recall capability ensures designers can recall their custom setup details.

Multiple Views

Multiple domain Views provide the necessary complete view of all supported interfaces' state, timing and protocol activity. Users can easily setup the analyzer to view timing, logic and protocol decode views to enable easy insights to the design. User can set different trigger conditions from the setup menu to capture timing and protocol activity at specific events. The decoded results can be viewed in timing, logic and protocol listing window with auto correlation. This comprehensive view of information makes it industry's best, offering an easy to use solution to debug the embedded interfaces protocol activity and analyze timing issues. Multiple cursors help designers to look into details of their design performance.

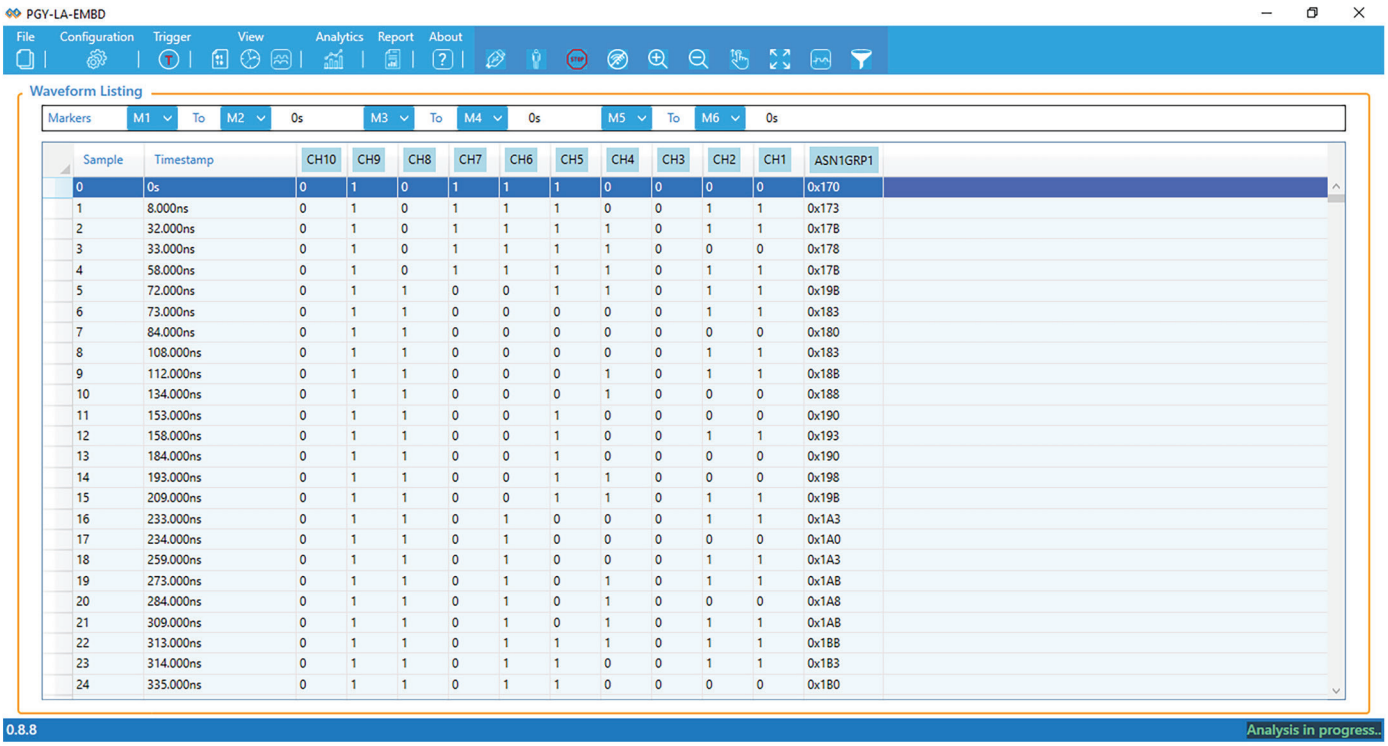
Timing View



Timing view is a unique capability of the PGY-LA-EMBD which enables designers to get detailed insights to their signals timing information. The timing view uses internal clock signal to plot the waveform. The flexible sampling rate selection enables designers to investigate Glitches which can cause issues in the functioning of their designs. Grouping feature enables designers to group various related signals for better viewing and analysis. Marker and Zoom features make it convenient to analyze any timing errors.

Ability to analyze any point in the captured data record ensures easy debug and analysis over a long capture duration.

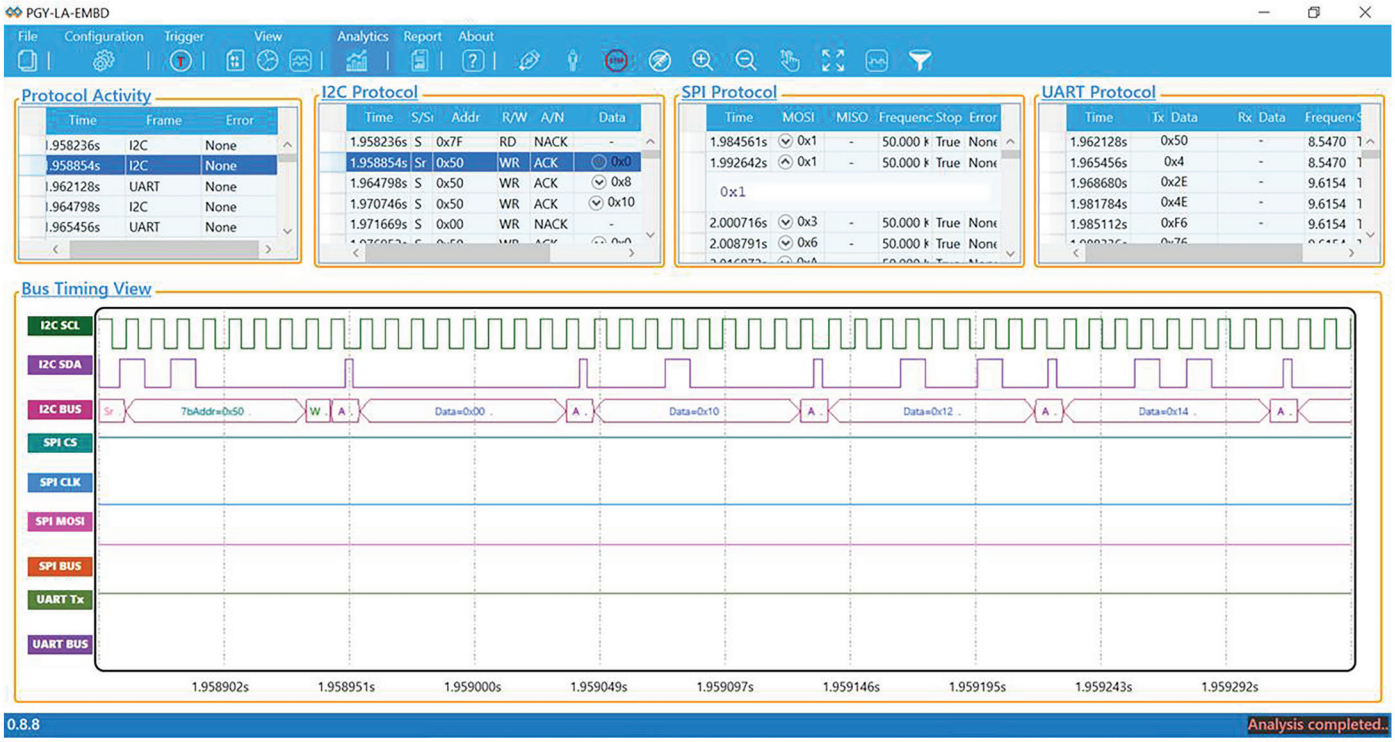
State View/Waveform Listing View



Sample	Timestamp	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	ASN1GRP1
0	0s	0	1	0	1	1	1	0	0	0	0	0x170
1	8.000ns	0	1	0	1	1	1	0	0	1	1	0x173
2	32.000ns	0	1	0	1	1	1	1	0	1	1	0x17B
3	33.000ns	0	1	0	1	1	1	1	0	0	0	0x178
4	58.000ns	0	1	0	1	1	1	1	0	1	1	0x17B
5	72.000ns	0	1	1	0	0	1	1	0	1	1	0x19B
6	73.000ns	0	1	1	0	0	0	0	0	1	1	0x183
7	84.000ns	0	1	1	0	0	0	0	0	0	0	0x180
8	108.000ns	0	1	1	0	0	0	0	0	1	1	0x183
9	112.000ns	0	1	1	0	0	0	1	0	1	1	0x18B
10	134.000ns	0	1	1	0	0	0	1	0	0	0	0x188
11	153.000ns	0	1	1	0	0	1	0	0	0	0	0x190
12	158.000ns	0	1	1	0	0	1	0	0	1	1	0x193
13	184.000ns	0	1	1	0	0	1	0	0	0	0	0x190
14	193.000ns	0	1	1	0	0	1	1	0	0	0	0x198
15	209.000ns	0	1	1	0	0	1	1	0	1	1	0x19B
16	233.000ns	0	1	1	0	1	0	0	0	1	1	0x1A3
17	234.000ns	0	1	1	0	1	0	0	0	0	0	0x1A0
18	259.000ns	0	1	1	0	1	0	0	0	1	1	0x1A3
19	273.000ns	0	1	1	0	1	0	1	0	1	1	0x1AB
20	284.000ns	0	1	1	0	1	0	1	0	0	0	0x1A8
21	309.000ns	0	1	1	0	1	0	1	0	1	1	0x1AB
22	313.000ns	0	1	1	0	1	1	1	0	1	1	0x1BB
23	314.000ns	0	1	1	0	1	1	0	0	1	1	0x1B3
24	335.000ns	0	1	1	0	1	1	0	0	0	0	0x1B0

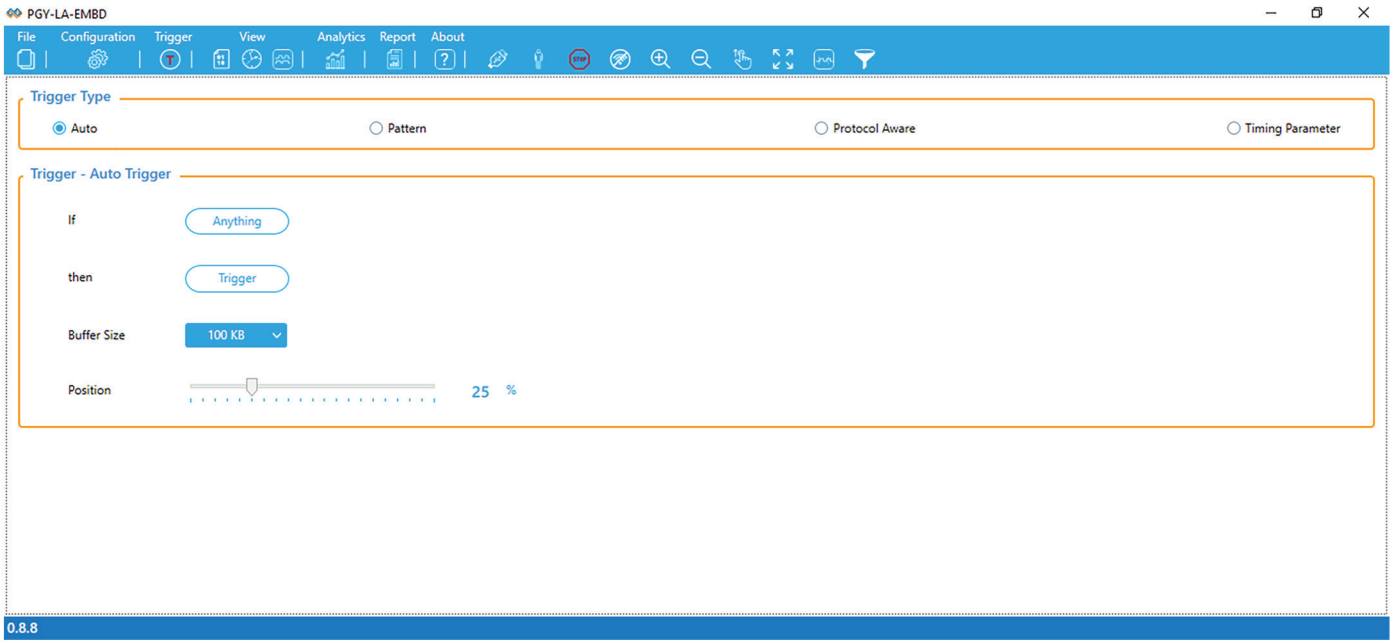
State view helps designers to see the actual signal behavior. Using the device clock as reference, it provides the plot of clock and data signals with bus diagram. Grouping of signals ensures designers have the flexibility to view signals together. All signals are time correlated to help look into setup and hold times, pulse width, missing data etc. which are very critical for digital designs as designers look to optimize their codes.

Protocol Decode View



Protocol Activity window provides the decoded packet information in each state and all packet details with error info in the packets. This gives the system level insight to the design teams. The individual protocol decodes windows based on selected interfaces ensures easy viewability for design teams. Selected frame in Protocol listing window will be auto correlated in timing view to view the timing information of the packet. Protocol errors will be highlighted to ensure designers are alerted to the same easily.

Powerful Trigger Capabilities



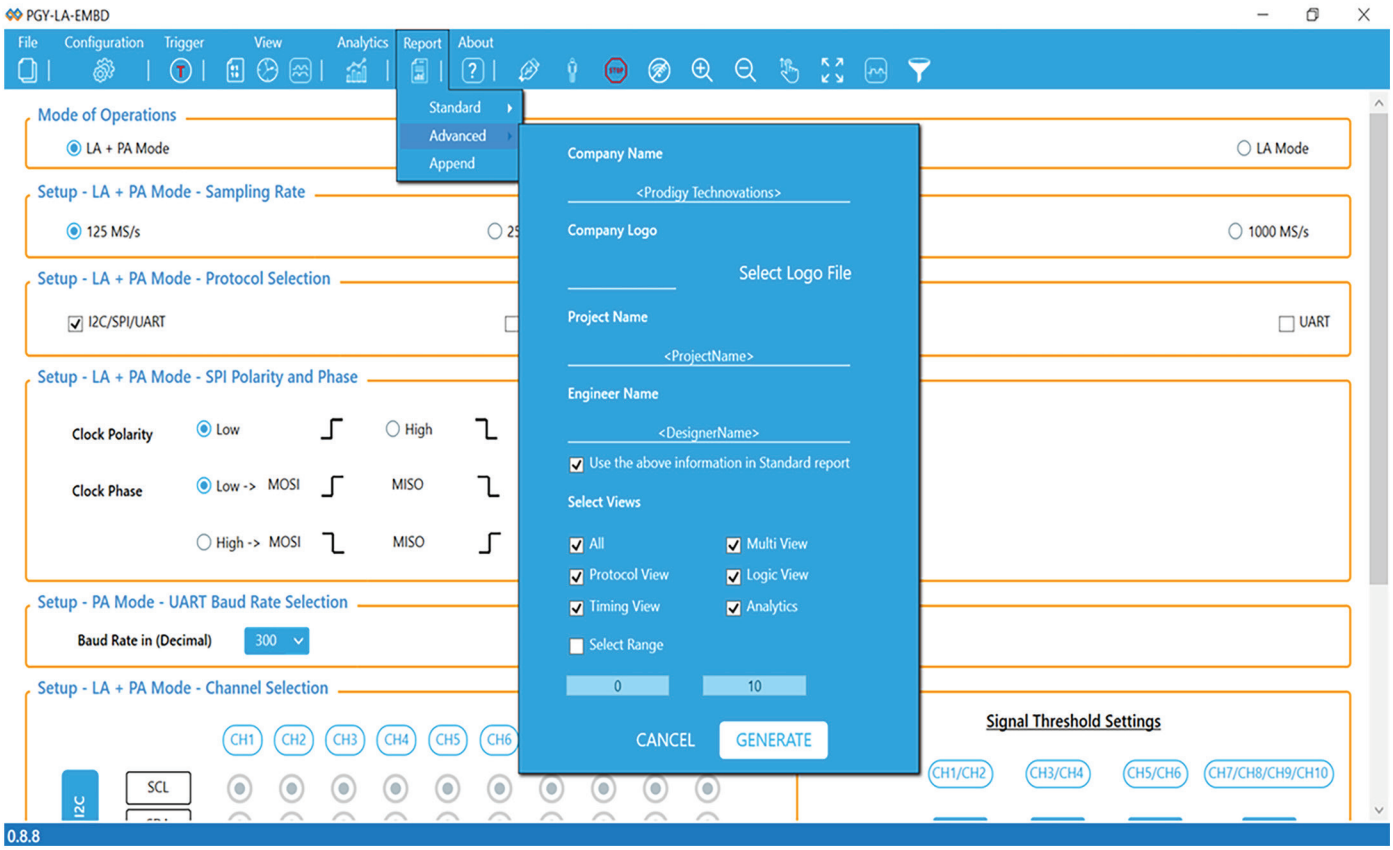
PGY-LA-EMBD supports Auto, pattern, Protocol aware and timing parameter trigger capabilities. Users can trigger on any of the Protocol packets. Comprehensive Trigger provides the flexibility to monitor different conditions.

Analytics

Detailed analytics on various protocol to enable better analysis and provide additional insights to designers.

Report

Report can be generated in PDF or CSV format with details of all the signal information, plots and custom details like name of the company, logo, tester name, date and time to ensure designers can document all details and share the report.



Specifications

PGY-LA-EMBD Specification	Features
Channels	Max 10 channels Logic Channels
State Speed	100MS/S (Synchronous capture)
Number of State clock support	Two. Flexibility to sample at rising or falling edge
Timing Speed	Up to 1GS/S (Asynchronous capture)
Record Length	Smart Continuous streaming of data to HDD/SSD of host computer
Voltage level support	0 to 5V, Flexibility to define logic threshold
Waveform Plot	Plots waveforms with flexible configurable bus diagram
List View	List all the data samples at each sampling point
Trigger for LA	Pattern Trigger, pulse width trigger, delay trigger
Protocol Decode Support	I2C, SPI, UART
Simultaneous decoding of I2C, SPI, UART	**Yes.** Connect I2C, SPI and UART bus to Logic Analyzer. Simultaneously captures the bus data and displays it in time correlated view with corresponding time waveforms
Protocol View with timing view (PA+Sys)	Displays the protocol decoded data with high sample rate timing waveform at the same time
API Support	Support for Automation of operation using Python or C++
Connector type	Flying Lead probe cable, female.#10 clip-on banana connectors as optional accessories.
External Triggers	Trigger Out SMA connector
Markers	SIX markers with delta information between two markers.
Views	Timing View State/Logic/Waveform Listing View Protocol View Bus-Diagram to display Protocol packets with timing diagram plot
Protocol Trigger	Auto (Trigger on any packet)- Default Pattern trigger Protocol aware trigger- **UART:** Start bit ,Parity Bit, Data **SPI :** Clock, Chip Select, MOSI Data, MISO data **I2C:** Start bit, Address, Data, Address plus Data, Ack, Nack, Repeated Start, Stop bit **Timing parameter trigger:** Pulse width (Positive or Negative) in ns. Delay Trigger
Capture duration	Smart streaming of Protocol Data to host HDD/SSD
Report	Report in PDF, CSV formats
Host Connectivity	USB 3.0
Dimensions	140mmx100mmx35mm
Weight	200 gms

Ordering Information

PGY-LA-EMBD (v 1.0): Logic Analyzer for Embedded Interfaces

Deliverables For PGY-LPA-EMBD

PGY—LA-EMBD Unit
USB3.0 cable
PGY-LA-EMBD Software in CD
Flying lead probe cable with female connector to connect to DUT

Optional Accessories

PGY-LA-EMBD-Cable: Flying lead probe cable with female connector to connect to DUT
PGY-LA-EMBD banana clips (set of #10)

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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical Layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.