PGY-SSM SD/SDIO/eMMC Protocol Analyzer is the comprehensive Protocol Analyzer with multiple features to capture and debug communication between host and memory under test. PGY-SSM Protocol Analyzer supports SD, SDIO and eMMC for data rates up to 200MHz DDR mode. PGY-SSM is industry’s first eMMC protocol analyzer that supports version 4.41, 4.51, 5.0 and 5.1 specifications. The innovative active probe has minimum electrical loading on the device under test (DUT) and allows protocol data capture without affecting the performance of the DUT. In an industry-first feature, PGY-SSM protocol analyzer allows continuous streaming of protocol data from PGY-SSM Protocol Analyzer to the host system (using USB3.0 or GbE interface) running the UI. Comprehensive decoding of protocol data, command units, and real-time error analysis enable effective verification of communication of SD/SDIO/eMMC host and device.

PGY-SSM Protocol Analyzer enables design and verification engineers to test and debug SD, SDIO and eMMC by triggering on command, response, data or CRC errors. It also provides instantaneous decoding of Command, Response, CID, CSD and Ext CSD registers. The Analytics feature offers easy to analyse graphical representation of command, response, data and frequency of operation for the acquired duration.
Key features and benefits:

- Continuous monitoring of protocol data for long time to capture elusive events (more than 30GB data capture)
- Analysis of captured data per standards for protocol integrity, count of data bursts, CMD CRC errors, Response CRC errors, Data CRC errors, Timing Values and Reserved commands
- Hardware-based protocol-aware trigger capability in real time enables capturing specific Events. Triggering facility on patterns, commands or error events.
- User can identify the anomalies by decoding command and response arguments
- Analytics feature provides analysis of acquired protocol data by plotting command, response, data and frequency of operation over acquired time
- Analytics feature also provides the decoding of device registers for easy analysis
- Filters allow you to view specific packets in decoded protocol packets
- Search feature for specific events in protocol activity
- Easy-to-use user interfaces saves time on learning curve
- Handles long duration capture and displays the decoded data without demanding extensive resources in host computer
- Inserting markers [using Trigger-In] in protocol activity helps in correlating the input digital signal with Protocol Activity
- Trigger-out signal for any specific protocol event allows triggering of other instruments such as oscilloscope
- Interface to host system [running UI] using USB3.0 or Gigabit Ethernet interface
- Flexibility to upgrade the hardware firmware using GbE interface provides easy field upgradation of firmware
- Export of Decoded data packets to txt file for further analysis

Specifications:

| Interfaces Supported | SD3.0 (UHS-I), SDIO4.0 and eMMC 4.41/4.51/5.0/5.1 Specifications |
| Protocol Decode      | Command, Response, CRC, Data, Boot Data, Arguments, Device registers |
| Data Decode          | 1 bit, 4 bit, 8 bit SDR or 4,8 bit DDR. |
| Protocol Test        | Protocol Integrity, CRC Errors, Timing values, Data CRC Errors, Reserved commands |
| Operating Voltage levels | 1.8V, 3.3V |
| Storage Capability   | Continuous streaming of protocol activity upto 30GB or 4 to 5 hour capture duration |
| Capture Mode         | Manual Run/Stop, Time specific |
| Capture Duration time| 1 sec to 5 hours |
| Trigger on           | Command, Response, CRC errors, Sequential trigger |
| Trigger Actions      | Capture data and/or trigger out signal |
| Signal Input         | Digital Signal input to mark the activities in Protocol activity |
| Host System Interface| USB3.0 or GbE interface |
Setup
PGY_SSM Protocol Analyser works on the principle of fat-pipe analysis where the analyser probes are connected on the interface bus between host and device[memory] of the unit under test. It captures all transactions that are going on between the host/device and does real time analysis for errors + a detailed analysis on the captured data which is made available through UI running on a host system. Captured data is stored in the hard disk of the system running UI, enabling a long capture [expect to have enough free space in the hard disk].

PGY-SSM Protocol Analyzer interfaces to host using USB3.0 (Super Speed) and GbE. PGY-SSM analyser & UI software runs in the host machine. PGY-SSM protocol analyzer also has the capability to capture boot data for eMMC.

Probing:
PGY-SSM Protocol Analyzer has active probe, which provides very flexible probing with minimum electrical loading of DUT. This specifically designed keeping to address challenges in probing eMMC/SD/SDIO signals. Probe supports 200MHz DDR bandwidth so that eMMC/SD/SDIO signals can be captured without any error. Probes has a flying probe lead set with berg post connector and solder able probe tips make it very convenient to connect to DUT.

Comprehensive Protocol Analysis:
PGY-SSM Software provides the industry’s best protocol analysis capabilities. A simple-to-use interface reduces the complexities and time for protocol debug. Time stamped view of decode listing provides a complete view of protocol activities between host and device. By clicking on selection prompts, the user can get the decode of arguments, CSD, CID registers, data activities and more [detailed view].

Protocol data capture and trigger:
PGY-SSM Protocol Analyzer has powerful protocol aware trigger capabilities allows capture protocol events at specific events. PGY-SSM supports simple and advanced trigger capabilities. PGY-SSM can trigger specific command, response, CRC error condition. Advanced trigger capabilities allows sequential trigger condition to capture protocol data after a sequence of events. In Auto mode, data is captured on pressing the RUN Button.

Protocol data capture duration is controlled by manual stop or setting the capture duration. Manual stop offers flexibility of set protocol data capture by visual activities in DUT. In time duration user set data capture in secs to 3 to 4 hours. During the capture mode, protocol data is continuously streamed to host system hard disk drive to storage.
Analytics:

a) Analytics features quickly provide insight into protocol activity without going through the complete protocol activity. As ample plot is shown below.

![Analytics plot](image1)

The Analytics view is a bird’s eye view of protocol activity for the captured long duration data. It reduces analysis time by viewing plot command, response, data and frequency of operation of captured data. The user can search for specific command or response in the plot.

b) Card/Device Information

![Card information](image2)

Card information provides decoding of register argument of device. Now the user no longer needs to manually decode each register value.

Host Machine Minimum Requirements

Microsoft Windows® 8, Windows 7, 16GB of RAM; Storage with at least 50 GB HDD space for the storing the acquired data Display with resolution of at least 1024x768

Ordering information:

PGY-SSM SD, SDIO and eMMC Protocol Analyzer
(Shipment includes Hardware, software CD, one set probe, USB3.0 and Ethernet Cable, power adopters)

Options:

PGY-SSM –S/W offline SD, SDIO, eMMC Protocol Analysis Software
(Shipment includes software CD with USB key for license)

Warranty:

Hardware and software carries warranty of one year. Probes are covered three month warranty for any manufacturing defects.

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